Program Details

Monday, 2 June 2025

8:30 - 9:00 **4F Main Hall**

Opening Session

Opening Remarks
Ichiro Omura, General Chair (*Kyushu Institute of Technology, Japan*)

ISPSD 2024 Ohmi Best Paper Award
Nando Kaminski, General Chair of ISPSD 2024 (*University of Bremen, Germany*)
Ulrike Grossner, Technical Program Committee Chair of ISPSD 2024 (*ETH Zurich, Switzerland*)

Program Introduction
Yuichi Onozawa, Technical Program Committee Chair (*Fuji Electric, Japan*)

9:00 -10:20 **4F Main Hall**

Plenary Session

Chairs: Ichiro Omura (*Kyushu Institute of Technology, Japan*) David Sheridan (*Alpha & Omega Semiconductor, USA*)

9:00 - 9:40 **Gallium Nitride: Past, Present and Future in an Ever-Changing Market**
Umesh Mishra (*ECE Department, UC Santa Barbara, CA, USA*)

9:40 -10:20 **Chuo Sinkansen with Superconducting Maglev and Semiconductor Power Conversion**
Junichi Kitano (*Central Japan Railway Company, Tokyo, Japan*)

10:20 -10:50 **3F A1/A2 Room and Foyer (Exhibition Area)**

Coffee Break

10:50 -12:30 **4F Main Hall**

HV-1: New Power Device Designs and Gate Control Method

Chairs: Wentao Yang (*HUAWEI Technologies, China*) Karthik Padmanabhan (*Alpha & Omega Semiconductor, USA*)

10:50 -11:10 **Shallow Active Trench CSTBT™ with Low Switching Loss for 6.5kV Class**
Kakeru Otsuka, Ayanori Gatto, Koji Tanaka, Shinya Soneda
Power Device Works, Mitsubishi Electric, Fukuoka, Japan

11:10 -11:30 **Influence of IGBT Switching Behavior on Conducted and Radiated Emissions below 30 MHz**
Yosuke Sakurai[1], Yasutoshi Yoshioka[2], Marco A. Azpúrua[3], Jordi Solé-Lloveras[3], Rik W. De Doncker[4]
[1]Semiconductors Business Group, Fuji Electric, Matsumoto, Japan; [2]Corporate R&D Headquarters, Fuji Electric, Tokyo, Japan
[3]EMC Electromagnetic BCN, S.L., Barcelona, Spain
[4]Institute for Power Electronics and Electrical Drives, RWTH Aachen University Aachen, Germany

11:30 -11:50 **First demonstration of 6.5kV fully scaled IGBT with ultra-shallow edge termination (USET)**
Takuya Saraya[1], Kiyoshi Takeuchi[1], Kazuo Itou[1], Toshihiko Takakura[1], Munetoshi Fukui[1], Shinichi Suzuki[1], Hiroyuki Takase[1], Wataru Saito[2], Shin-Ichi Nishizawa[2], Toshiro Hiramoto[1]
[1]The University of Tokyo, Tokyo, Japan; [2]Kyushu University, Fukuoka, Japan

11:50 -12:10 **A Novel 4.5 kV nonlatching IGCT for turn-on di/dt controllability without a clamp circuit**
Gurunath Vishwamitra Yoganath[1], Jan Fuhrmann[1], Tobias Wikström[2], Hans-Günter Eckel[1]
[1]Institute for Electrical Power Engineering, University of Rostock, Germany; [2]Hitachi Energy, Semiconductors, Switzerland

12:10 -12:30 **New Bidirectional Asymmetric High Voltage TVS (Transient Voltage Suppressor) device**
Boris Rosensaft[1], Xingchong Gu[2], Martin Schulz[3]
[1]SBU Bipolar Chip R&D, IXYS Global Services GmbH, Lampertheim, Germany; [2]PI&NPD Littelfuse Semiconductor, Wuxi, China
[3]Semiconductor Power Applications, Littelfuse Europe GmbH, Bremen, Germany

12:30 -14:00 **2F Civic Hall**

Lunch Break

Monday, 2 June 2025

14:00 -15:40 4F Main Hall

SiC-1: Performance of Superjunction SiC devices

Chairs: Ulrike Grossner (*ETH Zurich, Switzerland*) Noriyuki Iwamuro (*University of Tsukuba, Japan*)

14:00 -14:20 **Avalanche and Short Circuit Withstand Capabilities in 3.3 kV-class SiC Superjunction MOSFET**
Shinichiro Matsunaga[1], Takeshi Tawara[2], Syunki Narita[2], Masakazu Baba[2], Kensuke Takenaka[1], Tadao Morimoto[1], Shinsuke Harada[1]
[1]Advanced Power Electronics Research Center, AIST, Tsukuba, Japan; [2]Fuji Electric, Matsumoto, Japan

14:20 -14:40 **Bipolar characteristics of 3.3kV-class 4H-SiC Epi-refilled Super-Junction Diodes**
Haoyuan Cheng[1], Hengyu Wang[1], Chi Zhang[1], Jiangbin Wan[1], QianQian Que[1], Han Wang[1], Haoyu Wang[1], Ce Wang[1], Jingrui Han[2], Hungkit Ting[2], Kuang Sheng[1]
[1]College of Electric Engineering, Zhejiang University, Hangzhou, China; [2]Tianyu Semiconductor, Guangdong, China

14:40 -15:00 **Comparative Study on Charge-Imbalance Super Junction Termination for 3kV 4H-SiC Full-SJ and Semi-SJ Devices**
Chi Zhang[1], Hengyu Wang[1],Haoyuan Cheng[1], Jiangbin Wan[1], Han Wang[1], Haoyu Wang[1], Ce Wang[1], Zijian Hu[1], Jingrui Han[2], Hungkit Ting[2], Kuang Sheng[1]
[1]College of Electrical Engineering, Zhejiang University, Hangzhou, China; [2]Tianyu Semiconductor, Guangdong, China

15:00 -15:20 **Investigation of static and dynamic behavior of silicon carbide semi-super-junction structure in Schottky barrier diodes**
Hiroshi Kono, Katsuhisa Tanaka, Tsutomu Kiyosawa, Kenya Sano
Toshiba Electronic Devices & Storage, Hyogo, Japan

15:20 -15:40 **Comparative Study of Different Layouts for 1.7kV Charge-Balance-Assisted SiC MOSFETs**
Yuhan Duan[1,2], Botao Sun[3], Yuanlan Zhang[3], Pan Liu[1,2], Guangyin Lei[1], Min Li[1], Qingchun Jon Zhang[1]
[1]Academy for Engineering and Technology, Fudan University, Shanghai, China
[2]Research Institute of Fudan University in Ningbo, Ningbo, China; [3]SiChain Semiconductors (Ningbo), Ningbo, China

15:40 -16:10 **3F A1/A2 Room and Foyer (Exhibition Area)**
Coffee Break

16:10 -17:50 4F Main Hall

GaN-1: Novel GaN Power Device and Technologies 1

Chairs: Tom Chun-Lin Tsai (*TSMC, Taiwan*) Akira Nakajima (*AIST, Japan*)

16:10 -16:30 **First Demonstration of Optically-Controlled 650 V Power GaN HEMT with Ultrafast Switching Speed**
Xin Yang[1], Liyang Jin[2], Matthew Porter[3], Hongchang Cui[1], Zineng Yang[1], Hehe Gong[1], Han Wang[1], Linbo Shao[2], Yuhao Zhang[1]
[1]Department of Electrical and Electronic Engineering, The University of Hong Kong, Hong Kong, China
[2]Bradley Department of Electrical and Computer Engineering, Virginia Tech, Blacksburg, USA
[3]Center for Power Electronics Systems (CPES), Virginia Tech, Blacksburg, USA

16:30 -16:50 **First Demonstration of a Fully-Vertical GaN Power finFET with Direct Optical Triggering**
Jung-Han Hsia[1], Joshua Andrew Perozek[1], Joseph Park[2], Tomás Palacios[1]
[1]Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, MA, USA
[2]MIT Lincoln Laboratory, Lexington, MA, USA

16:50 -17:10 **Enhanced Photon-Generated Hole Spreading in p-GaN Gate Double-Channel HEMT for Suppression of Back-Gating Effect from Si Substrate**
Zheng Wu, Tao Chen, Yat Hon Ng, Haochen Zhang, Zongjie Zhou, Yan Cheng, Hang Liao, Yutao Geng, Yumeng Huang, Kevin J. Chen
Dept. of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong, China

17:10 -17:30 **Low $R_{ON}Q_G$ 1.2 kV-Class Normally-Off GaN Gate Injection Transistor on GaN Substrate with Asymmetric Gate Structure**
Hiroyuki Handa, Naohiro Tsurumi, Masao Kawaguchi, Masahiro Ogawa, Daisuke Shibata, Yoshio Okayama, Satoshi Tamura
Manufacturing Innovation Division, Panasonic Holdings, Osaka, Japan

17:30 -17:50 **Beyond 650 V Dynamic Switching of High Voltage AlGaN/GaN/AlN HEMTs on monocrystalline AlN Substrates**
Houssam Halhoul[1], Mihaela Wolf[1], Frank Brunner[1], Sven Besendörfer[2], Martin Damian Cuallo[1], Steffen Breuer[1], Gleb Lukin[2], Andreas Lesnik[2], Elke Meissner[2], Oliver Hilt[1]
[1]Ferdinand-Braun-Institut (FBH), Berlin, Germany
[2]Fraunhofer Institute for Integrated Systems and Device Technology IISB, Erlangen, Germany

18:00 -20:00 **2F Civic Hall**
Welcome Reception

Tuesday, 3 June 2025

8:40 - 10:20 **4F Main Hall**

LVT: Low Voltage Power Devices

Chairs: Atsushi Sakai (*Renesas Electronics, Japan*) Raffaella Roggero (*STMicroelectronics, Italy*)

8:40 - 9:00 **Current Sharing in Trench MOSFETs During Fast Switching Transients**

Riccardo Tambone[1,2], Alessandro Ferrara[1], Filippo Magrini[3], Raymond J.E. Hueting[2]

[1]Infineon Technologies Austria AG, Villach, Austria; [2]University of Twente, Enschede, The Netherlands

[3]Infineon Technologies AG, Neubiberg, Germany

9:00 - 9:20 **Polysilicon trench diode based on P-N junction**

Lia Masoero[1], Rosalia Germana[1], Adriano Novarese[1], Alfio Scuderi[2], Monica Petralia[2], Alessandro Nodari[1], Patrick Calenzo[1]

[1]Digital & Smart Power Techn. & Digital FE Manuf., VIPower R&D, STMicroelectronics, Rousset, France

[2]Analog & Power Front-End Manufacturing, STMicroelectronics, Catania, Italy

9:20 - 9:40 **Segmented Centroid and Stress-buffered P-body Taps for Stable Multi-finger Power CMOS**

JungHyun Oh[1,2], JungKyung Kim[3], JaeHong Jeong[3], Hoon Chang[3], OhKyum Kwon[3], SoYoung Kim[4]

[1]Department of Semiconductor and Display Engineering, Sungkyunkwan University, Suwon, Korea

[2]Samsung Institute of Technology, Samsung Electronics, Yongin, Korea; [3]Foundry Business, Samsung Electronics, Yongin, Korea

[4]Department of Semiconductor Systems Engineering, College of Information and Communication Engineering, Sungkyunkwan University, Suwon, Korea

9:40 -10:00 **Charge Field Modulation Mechanism and Its Experiments in SJ-Based SOI BCD process**

Wentong Zhang[1], Jiangnan Mu[1], Teng Liu[1], Nailong He[2], Liqi An[2], Jingchuan Zhao[2], Sen Zhang[2], Ping Li[3], Rongyao Ma[3], Yongqiang Cai[4], Ming Qiao[1], Zhaoji Li[1], Bo Zhang[1]

[1]State Key Laboratory of Electronic, Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu, China; [2]Technology Development Department, CSMC Technologies, Wuxi, China

[3]China Resources Microelectronics, Chongqing, China; [4]Beijing Normal University, Beijing, China

10:00 -10:20 **High Performance Producible 90nm CFP LDMOS with a Secondary DPN-ISSG FP**

Shaoxin Yu[1], Rongsheng Chen[1], Bo Wang[2], Xiaolong Zhao[2], Qishun Yao[2], Yan Jin[2]

[1]School of Microelectronics, South China University of Technology, Guangzhou, China

[2]R&D department, Runpeng Semiconductor Technology, Shenzhen, China

10:20 -10:50 **3F A1/A2 Room and Foyer (Exhibition Area)**

Coffee Break

10:50 -12:30 **4F Main Hall**

ICD: Power IC Design

Chairs: Jingshu Yu (*Intel, USA*) Wei-Jia Zhang (*Analog Device, USA*)

10:50 -11:10 **A Monolithic GaN IC with Temperature Compensated Active Clamp Driver and Short Circuit Protection for Wide Power Supply Range**

Yi Lu[1], Xin Ming[1, 2, 3], Yao Qin[1], Lin-min Chen[1], Chun-wang Zhuang[1], Xin-ce Gong[1], Wen-xi Lu[1], Bo Zhang[1]

[1]State Key Laboratory of Electronic, Thin Films and Integrated Devices, UESTC, Chengdu, China

[2]Shenzhen Institute for Advanced Study, UESTC, Shenzhen, China

[3]Institute of Electronic and Information of UESTC in Guangdong, Dongguan, China

11:10 -11:30 **Dynamic Reliability of IC-Interface GaN HEMTs Demonstrated under Ultra-Fast (ns), High-Frequency (MHz) Gate Overvoltage Stress (>30 V)**

Bixuan Wang[1], Qihao Song[1], Kalparupa Mukherjee[2], Loizos Efthymiou[2], Daniel Popa[2], Giorgia Longobardi[2], Dong Dong[1], Florin Udrea[2], Yuhao Zhang[3]

[1]Center for Power Electronics Systems (CPES), Virginia Tech, Blacksburg, USA; [2]Cambridge GaN Devices, Cambridge, UK

[3]Department of Electrical & Electronic Engineering, The University of Hong Kong, Hong Kong, China

11:30 -11:50 **12-V Tolerant Power-Rail ESD Clamp Circuit for Monolithic GaN-on-Silicon Integrated Circuits**

Chao-Yang Ke, Ming-Dou Ker

Institute of Electronics, National Yang Ming Chiao Tung University, Hsinchu, Taiwan

11:50 -12:10 **A Self-Powered Gate Driving Scheme Enabled by the GaN/SiC Cascode Power Device**

Ji Shu[1], Jiahui Sun[1,2], Mian Tao[3], Shi-Wei Ricky Lee[3], Kevin J. Chen[1]

[1]Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong, China

[2]College of Electrical Engineering, Zhejiang University, Hangzhou, China

[3]EPACK Lab, The Hong Kong University of Science and Technology, Hong Kong, China

12:10 -12:30 **Closed-Loop Active Gate Driver IC With Gate Current Control When Collector Current Equals Load Current**

Yaogan Liang, Yohei Sukita, Michihiro Ide, Makoto Takamiya

The University of Tokyo, Tokyo, Japan

12:30 -14:00 **2F Civic Hall**

Lunch Break

Tuesday, 3 June 2025

14:00 -15:20 4F Main Hall

GaN-2: GaN Power Device Reliability and Tests

Chairs: Yasuhiro Uemoto (*Infineon Technologies, Japan*) Roy K.-Y. Wong (*National Tsing Hua University, Taiwan*)

14:00 -14:20 **Dynamic Stability and Reliability of Multi-Kilovolt GaN Monolithic Bidirectional HEMT**

Yuan Qin[1], Yijin Guo[1], Matthew Porter[1], Ming Xiao[3], Hehe Gong[1], Zineng Yang[1], Daniel Popa[4], Loizos Efthymiou[4], Kai Cheng[5], Zhiqin Chu[2], Han Wang[2], Florin Udrea[4,6], Yuhao Zhang[2]

[1]Center for Power Electronics Systems, Virginia Tech, Blacksburg, VA, USA

[2]Department of Electrical and Electronic Engineering, University of Hong Kong, Hong Kong, China; [3]Xidian University, Xi'an, China

[4]Cambridge GaN Devices, Cambridge, UK; [5]Enkris Semiconductor, Suzhou, China; [6]University of Cambridge, Cambridge, UK

14:20 -14:40 **Verification of p-GaN Gate Lifetime Models through Wide Time-scale (μs-10^7 s) Measurement**

Sijiang Wu[1], Siyuan Ye[1], Jinjin Tang[1], Junting Chen[1], Shanshan Wang[1], Junlei Zhao[1], Zuoheng Jiang[1], Haohao Chen[1], Zheyang Zheng[2], Jun Ma[1], Mengyuan Hua[1]

[1]Department of Electronic and Electrical Engineering, Southern University of Science and Technology, Shenzhen, China

[2]School of Microelectronics, University of Science and Technology of China, Hefei, China

14:40 -15:00 **Ultrafast Junction Temperature Mapping During Surge Current Transient and Thermal Management in Vertical GaN PiN Diode**

Jiahong Du[1], Haobin Lin[2], Dazhi Hou[2], Shibing Long[1], Shu Yang[1]

[1]School of Microelectronics; [2]Department of Physics, University of Science and Technology of China, China

15:00 -15:20 **Mechanism of Leakage Current Degradation in p-GaN Gate HEMTs under Gamma Irradiation**

Zhao Wang[1], Qingchen Jiang[1], Shenghuai Liu[1], Xin Zhou[1], Huan Gao[1], Qi Zhou[1], Zhao Qi[1], Ming Qiao[1, 2], Bo Zhang[1]

[1]State Key Laboratory of Electronic, Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu, China

[2]Shenzhen Institute for Advanced Study, University of Electronic Science and Technology of China, Shenzhen, China

15:20 -15:40 **3F A1/A2 Room and Foyer (Exhibition Area)**

Coffee Break

15:40 -17:40 3F A3/A4 Room

LVT-P: Low Voltage Power Devices 2 (Poster Session)

A Novel Split Contact Field Plate LDMOS with a Floating Gate for Hot Carrier Degradation Improvement

Qiao Teng[1], Yongyu Wu[1,3], Kai Xu[1,2], Dawei Gao[1]

[1]College of Integrated Circuits, Zhejiang University, Hangzhou, China

[2]ZJU-Hangzhou Global Scientific and Technological Innovation Center, Zhejiang University, Hangzhou, China

[3]Zhejiang ICsprout Semiconductor, Hangzhou, China

Novel Optimization Method of Multi-Devices using TCAD Driven Machine Learning in BCD Process

Junhyeok Kim[1], Kyuyeop Lee[1], Yunjun Nam[1], Joohyung Yoo[1], Juwon Park[2], Dawon Jeong[1], Jaehyun Yoo[1], Yonghee Park[1], Dae Sin Kim[1]

[1]CSE team, Samsung Electronics, Hwasung-Si, Korea; [2]PA4 team, Samsung Electronics, Hwasung-Si, Korea

Chip Layout Optimization of Trench Length and the Upper Electrode Contact in Trench Field Plate MOSFET

Casey Clendennen[1], Tomoaki Shinoda[1], Shinpei Onishi[1], Hajime Kataoka[1], Masaki Nagata[2]

[1]Device Development Dept., ROHM, Kyoto, Japan; [2]Global IT Infrastructure Dept., ROHM, Kyoto, Japan

Irradiation Hardening of SGT Based on Combined IPO Structure and Mechanism Modeling of Leakage Current Optimization

Junyan Zhu[1], Haonan Liu[1], Jun Ye[1,3], Xuan Xiao[3,4], Ruihan Gao[1], Junfeng Yu[1], Xiaodong Yang[1], Zhuang Wang[1], Chunlei Wu[1], Weiye Mo[3], Hongping Ma[5], Qingchun Zhang[5], Liang Li[6], Qingdong Zhang[7], Tao Wang[7], Wei Huang[2], David Wei Zhang[1]

[1]Shanghai Institute of Intelligent Electronics & Systems, School of Microelectronics, Fudan University, Shanghai, China

[2]School of Integrated Circuits, Jiangnan University, Wuxi, China; [3]Wuxi China Resources Huajing Microelectronics, Wuxi, China

[4]College of Physics, Sichuan University, Chengdu, China; [5]School of Academy of Engineering & Technology, Fudan University, Shanghai, China

[6]School of Electronic Information Engineering, Suzhou Vocational University, Suzhou, China; [7]Wuxi Microelectronics Scientific and Research Center, Wuxi, China

Integrated Fast-Recovery SGT-SBR Devices with Majority Carrier Modulation during Wide Temperature Range

Jun Ye[1,2], Haonan Liu[1], Ruihan Gao[1], Xuan Xiao[2,3], Junyan Zhu[1], Weiye Mo[2], Yang Song[2], Xiaodong Yang[1], Zhuang Wang[1], Jiao Liang[4], Hongping Ma[4], Qingchun Zhang[4], Wei Huang[5], ChunLei Wu[1], David Wei Zhang[1]

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[2]Wuxi China Resources Huajing Microelectronics, Wuxi, China; [3]College of Physics, Sichuan University, Chengdu, China

[4]Academy for Engineering & Technology, Fudan University, Shanghai, China; [5]School of Integrated Circuits, Jiangnan University, Wuxi, China

BCD HVpMOS with Double-Functional-RESURF to Improve HCI Reliability

Tomohiro Imai[1], Atsushi Sakai[1], Zen Inoue[2]

[1]Process Tech and PDK Department, Operations Engineering Division, Renesas Electronics, Ibaraki, Japan

[2]MCU Device Technology Department, Device Technology Division, Renesas Electronics, Kumamoto, Japan

Novel Multistack Floating Field Plate MOSFET and Image Clustering-based Design Analysis

Hiro Gangi[1], Yasunori Taguchi[1], Kentaro Takagi[1], Kouta Nakata[1], Kairu Yoshida[1], Taichi Fukuda[1], Hiroki Nemoto[1], Shotaro Baba[1], Yusuke Kobayashi[1], Tomoaki Inokuchi[1], Tatsuya Nishiwaki[2], Kenya Kobayashi[2]

[1]Corporate Research & Development Center, Toshiba, Kanagawa, Japan

[2]Advanced Semiconductor Device Development Center, Toshiba Electronic Devices & Storage, Kanagawa, Japan

Design and Performance Enhancement of Integrated Schottky Contact in Low-Voltage LDMOS on 55nm BCD Platform

Dingxiang Ma[1], Yuanqing Ye[2], Yangjie Liao[1], Jiawei Wang[1], Fanyi Zeng[2], Bo Zhang[1], Ming Qiao[1,2]
[1]*State Key Laboratory of Electronic, Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu, China*
[2]*Shenzhen Institute for Advanced Study, University of Electronic Science and Technology of China, Shenzhen, China*

High Reliability Tri-zone Heterogeneous Charge Balanced SJ-LDMOS with Novel Silicon Rich Oxide and Its Experimental Verification

Teng Liu[1,2], Hao Wang[2], Wentong Zhang[1], Nailong He[2], Shiyao Cai[1], Yuxiao Kun[1], Jiangnan Mu[1], Zhekai Hu[1], Ting Wang[2], Ziao Zhang[2], Liqi An[2], Yongshun Li[2], Huajun Jing[2], Liang Song[2], Sen Zhang[2], Yongsheng Sun[3], Hao Fang[3], Sheng Dong Hu[4], Ming Qiao[1], Zhaoji Li[1], Bo Zhang[1]
[1]*State Key Laboratory of Electronic, Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu, China*
[2]*Technology Development Department, CSMC Technologies, Wuxi, China*
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15:40 -17:40 3F A3/A4 Room

ICD-P: Power IC Design 2 (Poster Session)

An On-Chip Tunable Negative Power Supply within SiC MOSFET Gate Driver for Spurious Conduction Suppression and Reliable Driving

Yun Dai, Zekun Zhou, Rongxing Lai, Zijun Zhou, Jiaxing Mao, Bo Zhang
State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu, China

A Study on a 4H-SiC-Based ESD Protection Device with lower Operating Voltage Using an Additional PNP BJT Structure

U-Yeol Seo[1], Jae-Yoon Oh[1], Min-Seo Kim[1], Dong-Hyun Kim[1], Ji-Hye Yoo[1], Hee-Bae Lee[2], Seung-Hyun Kim[2], Kyu-Hyun Jung[2], Yong-Seo Koo[3]
[1]*Dept. Engineering of Foundry, DanKook University, Yongin, Korea;* [2]*Tech Development Team3, DB HiTek, Bucheon, Korea*
[3]*Dept. Engineering of Electronics and Electrical, DanKook University, Yongin, Korea*

High Voltage Monolithic GaN Power IC with High Speed Low-power Consumption Level Shifter Circuit

Qianheng Dong[1], Jing Zhu[2], Yifei Zheng[1], Haoran Wang[1], Xiang Fan[1], Zihang Chen[1], Siyang Liu[1], Weifeng Sun[1], Kai Zhang[3], Siyuan Yu[4]
[1]*National ASIC System Engineering Research Center, Southeast University, Nanjing, Jiangsu, China*
[2]*Wuxi Institute of Integrated Circuit Technology, Southeast University, Wuxi, Jiangsu, China*
[3]*Nanjing Electronic Devices Institute, Nanjing, Jiangsu, China;* [4]*Wuxi Chipown Micro-electronics, Wuxi, China*

A Dynamic Gate Driver with Auto-Patterning to Reduce Ringing and Switching Loss

Wentao Cui[1], Wei-Jia Zhang[2], Jingyuan Liang, Haruhiko Nishio[3], Motomitsu Iwamoto[3], Wai Tung Ng[1]
[1]*The Edward S. Rogers Sr. Dept. of Electrical and Computer Engineering, University of Toronto, Toronto, ON, Canada*
[2]*Dept. of Electrical and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong, China*
[3]*Semiconductor Business Group, Fuji Electric, Matsumoto, Japan*

LLC Resonant Converter Controller with Burst Mode Control and Soft-Start Function

Shuang-Quan Tsai[1], Wan-Chien Chen[1], Chang-Ching Tu[2], Yi-Kai Hsiao[2], Hao-Chung Kuo[2], Po-Hung Chen[1]
[1]*Institute of Electronics, National Yang Ming Chiao Tung University, Hsinchu, Taiwan;* [2]*Hon Hai Research Institute, Hsinchu, Taiwan*

A High Precision and Robustness Isolated Analog Signal Sensing For Monitoring Power Stages

Yu-han Chen , Xin Ming, Yu-tong Wu ,Tian-yi Sun, Jun-yu Chen, Zhuo Wang, Bo Zhang
State key Laboratory of Electronic, Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu, China

15:40 -17:40 3F A3/A4 Room

GaN-P1: GaN Devices (Poster Session)

Dynamic Performance Analysis of GaN Digital Logic Gate Circuits for MHz-level Operation via CTL-based ICs Platform

Yang Jiang[1,2], Fangzhou Du[1], Ziyang Wang[1], Kangyao Wen[1], Mujun Li[1], Yifan Cui[1], Han Wang[2], Qing Wang[1], Hongyu Yu[1,3]
[1]*School of Microelectronics, Southern University of Science and Technology, Shenzhen, China*
[2]*Department of Electrical and Electronic Engineering, The University of Hong Kong, Pokfulam Road, Hong Kong*
[3]*School of Integrated Circuit, Shenzhen Polytechnic University, Shenzhen, China*

A Comprehensive Study on Device Reliability and Failure Mechanism of 650V p-GaN Gate HEMTs Under Long-Term HTRB Stress Beyond 150 °C

Lei Tang[1], Jinggui Zhou[1], Binju Qiu[1], Huan Gao[1], Jianggen Zhu[1], Kuangli Chen[1], Ning Yang[1], Bo Zhang[1], Qi Zhou[1,2]
[1]*School of Integrated Circuit Science and Engineering, University of Electronic Science and Technology of China, Chengdu, China*
[2]*Institute of Electronic and Information Engineering, UESTC, Dongguan, China*

Dependence of UIS Capability in GaN HEMTs on Substrate Bias and p-Gate Contacts

Wataru Saito, Shin-ichi Nishizawa
Research Institute for Applied Mechanics, Kyushu University, Fukuoka, Japan

Self-aligned p-GaN Gate Controlled Diodes With Tunable Forward Conduction/Reverse Blocking Properties For High Efficiency Buck Converter

Jinggui Zhou[1], Shuting Huang[1], Jianggen Zhu[1], Yuqi Liu[1], Enchuan Duan[1], Lei Tang[1], Wenzheng Liu[1], Xuan Li[1], Peng Luo[3], Yong Liu[3], Qi Zhou[1,2], Bo Zhang[1]
[1]*School of Integrated Circuit Science and Engineering, University of Electronic Science and Technology of China, Chengdu, China*
[2]*Institute of Electronic and Information Engineering, UESTC, Dongguan, China;* [3]*Nanjing Dan Xi Technology, China*

Impact of Substrate Termination on the Performances of Monolithic ESD Protection Circuit Using Bidirectional GaN HEMTs

Yanfeng Ma[1], Sheng Li[1], Hao Yan[1], Lixi Wang[1], Mingfei Li[1], Weihao Lu[1], Jie Ma[1], Ran Ye[1], Denggui Wang[2,3], Jianjun Zhou[2,3], Wangran Wu[1], Jiaxing Wei[1], Long Zhang[1], Siyang Liu[1], Weifeng Sun[1]
[1]*National ASIC System Engineering Research Center, Southeast University, Nanjing, China*
[2]*State Key Laboratory of Wide-Bandgap Semiconductor Devices and Integrated Technology &* [3]*Nanjing Electronic Devices Institute, Nanjing, China*

Tuesday, 3 June 2025

High-Vth E-Mode PIN-Gate GaN HEMT : Supporting Gate Drive Voltages >12 V

Mao Jia, Bin Hou, Ling Yang, Xuefeng Zheng, Xiaohua Ma, Yue Hao
National Engineering Research Center of Wide Band-gap Semiconductor, Xidian University, Xi'an, China

Monolithic Heterogeneous Integration of 6-Inch GaN/Si CMOS 1P2M Process on Si (111) Substrate and Platformed Devices

Wenzhang Du[1], Hanzhao He[1], Xiaojun Fu[7], Wenqi Fan[1], Junyan Zhu[1], Junfeng Yu[1], Xiaodong Yang[1], Haonan Liu[1], Zhuang Wang[1], Ruihan Gao[1], Jiao Liang[3], Hongping Ma[3], Qinchun Zhang[3], Wang Ma[4], Li Yuan[4], Zhaojun Liu[5], Guangsheng Zhang[7], Chen Qian[7], Yuan Wang[8], Yue-Chan Kong[8], HaiOu Li[9], Tao Wang[6], Liang Li[10], Yuan-Yang Xia[11], Yi-Heng Li[11], Ting Gang Zhu[11], Shujun Cai[6], Wei Huang[2], David Wei Zhang[1]
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Enhanced Irradiation Capability in AlGaN/GaN p-GaN-Hybrid Anode Power Diodes via Structural Hardening Design

Feng Zhou[1,2], Tianyang Zhou[1], Tianqi Wang[3], Peipei Hu[4], Pengfei Zhai[4], Jie Liu[4], Zhichao Wei[5], Yuanyang Xia[6], Leke Wu[6], Ke Wang[6], Yiheng Li[6], Tinggang Zhu[6], Weizong Xu[1], Dunjun Chen[1], Rong Zhang[1], Hai Lu[1]
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Physical Model of Trapping-Induced Dynamic Degradation in GaN HEMT

Chih-Kai Chang[1], Chao-Ta Fan[1], Pao-Tin Lin[1], Yen-Chieh Huang[1], Po-Chin Peng[2], Cheng Chun Huang[2], Ming-Cheng Lin[1]
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Experiment and Simulation Study of Single-Event Burnout in GaN Event-Triggering HEMTs

Ruize Sun[1,2], Renjie Wu[1], Xiaoming Wang[3], Yun Xia[3], Chao Liu[1], Wanjun Chen[1,2], Bo Zhang[1]
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Comparison of Total Ionizing Dose Effects in GaN HEMTs with p-GaN Gate Structure and Cascode Configuration

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Reverse Recovery Loss in Monolithic GaN Half-Bridge Chip with P-N Junction Isolation

Mingfei Li[1], Sheng Li[1], Fenglei Song[1], Yanfeng Ma[1], Weihao Lu[1], Jianjun Zhou[2], Denggui Wang[2], Jie Ma[1], Ran Ye[1], Jiaxing Wei[1], Long Zhang[1], Siyang Liu[1], Weifeng Sun[1]
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Heavy-Ion Radiation-Induced Dynamic On-Resistance Degradation for P-GaN Gate HEMTs

Huan Gao[1], Xin Zhou[1], Zhao Wang[1], Wen Yang[2], Qi Zhou[1], Bo Zhang[1]
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Suppressed Substrate-Coupled Cross-Talk Effects in GaN-on-Sapphire Platform Under High-Temperature and High-Voltage Applications

Junsong Jiang[1], Bomin Jiang[2], Zhanfei Han[3], Yang Zhang[1], Mengdie Zhang[1], Xingang Ren[1], Xi Tang[1], Xiangdong Li[3], Shu Yang[2], Jincheng Zhang[3]
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On the Rational Extraction of the Channel Mobility of Schottky-Type p-GaN Gate Power HEMTs

Chi Wang[1], Zhisheng Nie[1], Hao Zhang[1], Yifang Zhang[1], Li Zhang[2], Mengyuan Hua[3], Shibing Long[1], Zheyang Zheng[1]
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A P-Channel GaN Insulated Gate Bipolar Transistor with Outstanding Current Capability

Mengyao Zhao[1], Jie Ma[1], Tianchun Nie[1], Qiwei Peng[1], Denggui Wang[2], Jianjun Zhou[2], Sheng Li[1], Jiaxing Wei[1], Siyang Liu[1], Long Zhang[1], Weifeng Sun[1]
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Engineering Extrinsic Resistance of E-Mode GaN p-FET towards Enhanced Current Density

Jialin Duan[1], Jingjing Yu[1], Teng Li[1], Hengyuan Qi[1], Sihang Liu[1], Yunhong Lao[1], Maojun Wang[1], Junchun Bai[3], Bin Cheng[3], Jinyan Wang[1], Bo Shen[2], Jin Wei[1]
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Improved Normally-off 1200 V GaN-on-Si MOS-HEMT with Novel AlGaN Back Barrier

Cédric Masante, Stéphane Bécu, Blend Mohamad, Aurélien Olivier, Florent Gréco, Rémi Riat, Simona Torrengo, Johnny Amiran, Romain Laviéville, Arnaud Anotta, Etienne Nowak
Univ. Grenoble Alpes, CEA, Leti, Grenoble, France

Investigation of Dynamic R_{ON} in p-GaN Gate HEMTs under Steady-State Soft-Switching: Roles of OFF-State Trapping and Hole Injections

Hongkeng Zhu, Elison Matioli
Power and Wide-Band-Gap Electronics Research Laboratory (POWERlab),
Institute of Electrical and Micro Engineering, École Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland

Tuesday, 3 June 2025

Demonstration of 3300-V GaN HEMTs on 6-inch Sapphire for Medium-Voltage Applications: A Cost Effective and High-Performance Solution

Junbo Wang[1], Xiangdong Li[1,2], Jian Ji[1], Lili Zhai[1], Lu Yu[1], Zhanfei Han[1], Tao Zhang[1,2], Xi Jiang[1,2], Song Yuan[1,2], Long Chen[3], Lezi Wang[3], Zilan Li[3], Weitao Yang[4], Chao Sheng[4], Shuzhen You[1,2], Yue Hao[1,2], Jincheng Zhang[1,2]

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Dynamic Threshold Voltage Extraction for GaN HEMT via a Source-Series-Connected Capacitor

Wenkang Ji[1], Ying Wang[1], Zhixing Zhao[2], Zilin Wu[1], Haifeng Zhan[2], Lekang Fan[1], Zesen Chen[1], Zuoran Luo[1], Tian Luo[1], Qianshu Wu[1], Jinwei Zhang[1], Zixin Wang[1], Yang Liu[1]

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A > 10 kV/2.1 GW/cm^2 AlGaN/GaN SBD with Current-Collapse Suppression via in-situ NH_3 Plasma Treated GaN Passivation

Jiahao Chen[1], Ruowei Liu[1], Tao Zhang[1], Shengrui Xu[1], Huake Su[1], Jinfeng Zhang[1], Zeyang Ren[1], Xiangdong Li[2], Hongchang Tao[1], Yue Hao[1], Jincheng Zhang[1]

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Realization of High-Voltage Depletion-mode HEMTs with Tunable Threshold Voltage on a Standard Enhancement-mode GaN Platform

Fengping Lin[1], Xiaoyu Liu[1], Zhiwen Dong[2], Junsong Jiang[1], Suxia Guo[1], Changhui Zhao[1], Zhaofu Zhang[3], Baikui Li[4], Gaofei Tang[2], Xi Tang[1]

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Dynamic On-Resistance Degradation in E-mode GaN HEMTs Under Over-Voltage Hard Switching Stress: Insight of Physical Space and Energy Levels

Haoran Wang[1], Po-Yen Huang[2], Wei-Ting Hsu[1], Shawn S. H. Hsu[1,2], Roy K.-Y. Wong[1,2]

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High-performance InAlN/GaN HEMTs and Monolithically Integrated Inverters enabled by InAlOxN1-x Plasma-Induced-Oxidation Charge Trapping Layer

Fangzhou Du[1], Yang Jiang[1,2], Ziyang Wang[1], Kangyao Wen[1], Mujun Li[1], Xiaohui Wang[1], Yi Zhang[1,2], Chenkai Deng[1], Qing Wang[1], Hongyu Yu[1,3]

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Dynamic Overvoltage and Energy Loss in p-GaN HEMTs under Ultraviolet Pulsed Laser-Induced Single Event Irradiation

Mai Zhang[1,2], Feng Zhou[1,2], Yijun Shi[3], Zhengxiang Tang[1], Can Zou[1,2], Weizong Xu[1], Dong Zhou[1], Fangfang Ren[1], Dunjun Chen[1], Rong Zhang[1], Hai Lu[1]

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Enhanced Single-Event Hardness in GaN-on-Si HEMT With Gate-Junction Termination Extension

Xuan Xie, Minze Wang, Ziang Wang, Zhi Wang, Chenyue Chu, Guangwei Xu, Shibing Long, Shu Yang

School of Microelectronics, University of Science and Technology of China, Hefei, China

Demonstration of High Voltage (>2000V) AlGaN/GaN Schottky Barrier Diode with p-GaN Anode Edge Termination and Cathode-connected p-GaN Islands for Enhanced Dynamic R_{ON} Stability

Hung-Chun Chen[1], Pei-Jung Wang[1], Hung-Wei Chen[2], Tian-Li Wu[1,2,3]

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Through-GaN-Via Design Rule Investigation of GaN Power HEMTs on Si Substrate

Longge Deng[1], Ji Shu[1], Jiahui Sun[1,2], Kevin J. Chen[1]

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Accurate Dynamic ON-resistance Characterization of Low-voltage GaN Power HEMTs

Yuwei Wu[1], Ji Shu[1], Jiahui Sun[1,2], Binghong Wang[1], Zongjie Zhou[1], Kevin J. Chen[1]

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[2]College of Electrical Engineering, Zhejiang University, Hangzhou, China

High performance p-GaN gate HEMT with TiN_xO_y resistive field plate structure

Zhuocheng Wang[1], Wanjun Chen[1], Fangzhou Wang[2], Cheng Yu[1], Xiaochuan Deng[1], Ping Yu[2], Zheyu Huang[1], Yang Wang[2], HaiQiang Jia[2,3], Hong Chen[3], Bo Zhang[1]

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On the Impacts of Mobility Mismatching-Induced Asymmetric Rising and Falling Edges in GaN-based CMOS Circuits for Prospective Power Integration

Yang Zhang, Haoran Tao, Junchen Huang, Xiaomin Wang, Shibing Long, Zheyang Zheng

School of Microelectronics, University of Science and Technology of China, Hefei, China

Expanded Gate-Voltage Operating range of p-GaN gate HEMTs Operated in Synchronized Photonic-Electronic Driving (SPED) Scheme

Longge Deng, Haochen Zhang, Zheng Wu, Yan Cheng, Tao Chen, Kevin J. Chen
Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong, China

High I_{ON}/I_{OFF} Ratio > 10^5 Ag-Gated E-Mode GaN p-FETs Enabled by p^{++}-GaN Contact and Polarization-Enhanced AlN Layer

Zhiwei Sun[1,2], Hao Tian[1,2], Weisheng Wang[1,2], Xuanming Zhang[1,2], Maoqing Ling[1,2], Jie Zhang[2,3], Yinchao Zhao[2,3], Harm van Zalinge[2], Ivona Z. Mitrovic[2], Kain Lu Low[1,2], Sen Huang[4], Wen Liu[1,2],
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Surge Current Operation of Power GaN HEMTs with p-GaN Gate Under Positive Gate Voltage

Maximilian Goller, Madhu Lakshman Mysore, Dezhi Yang, Mohamed Alaluss, Josef Lutz, Thomas Basler
Chair of Power Electronics, University of Technology Chemnitz, Chemnitz, Germany

A Highly Linear 2-Transistor Monolithic Temperature Sensor Employing p-GaN HEMTs for GaN Power ICs

Fangqing Li[1,2], Yifan Dong[1,2], Xinyu Sun[1,2], Haodong Wang[1,2], Xin Chen[2], Yaozong Zhong[2], Hongwei Gao[1,2], Haoran Qie[2], Tengfei Li[1,2], Gaofei Zhi[2], Yu Zhou[1,2], Qian Sun[1,2], Hui Yang[1,2]
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Dual- vs. Single-Peak Transconductance Evolution in Schottky p-GaN Gate HEMTs: Influence of Partially and Fully Depleted p-GaN layer

Xuan Liu, Chao Feng, Yuhao Wang, Xinyue Dai, Zuoheng Jiang, Keping Wu, Jiawei Chen, Danfeng Mao, Rongxing Du, Xiaoping Wang, Haolin Hu, Wei Zeng, David Zhou, Yuxi Wan
Shenzhen Pinghu laboratory, Shenzhen, China

15:40 -17:40 3F A3/A4 Room

GaN-P2: Vertical GaN Devices (Poster Session)

Enhancing Key Performance of Vertical p-NiO/n-GaN Heterojunction Diodes through Plasma Treatment and Oxygen Post-Annealing

Yeying Huang[1,2], Min Wang[1,2], Na Sun[3], Renqiang Zhu[4], Xiaohua Li[1], Jianbo Liang[5], Jiandong Ye[3], Chunfu Zhang[6], Hezhou Liu[1,2], Junfa Mao[2], Xinke Liu[1, 2]
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Enhancing Key Performance of Vertical GaN MOS Capacitors through GaO_x Interface Technology

Jinpei Lin[1,2], Xinyi Pei[3], Xiaohua Li[1], Haiwen Liu[2], Renqiang Zhu[4], Chunfu Zhang[5], Hsien-Chin Chiu[6], Jianbo Liang[7], Hezhou Liu[1,2], Junfa Mao[2], Xinke Liu[1, 2]
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Analysis of Acceptor Activation and Lateral Diffusion of Channeled-implanted Mg Atoms in Vertical GaN Junction Barrier Schottky Diodes

Kazuki Kitagawa[1], Tsutomu Uesugi[2], Masahiro Horita[1], Tetsu Kachi[2], Jun Suda[1]
[1]*Department of Electronics, Nagoya University, Nagoya, Japan*
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1500 V GaN-on-Si Vertical Power MOSFETs: from quasi-vertical to fully-vertical topology

Yuchuan Ma[1,2], Hang Chen[1,2], Shuhui Zhang[1,2], Xiangyu Teng[1,2], Xiaoping Meng[1,2], Huantao Duan[3], Bin Hu[3], Huimei Ma[3], Jianfei Shen[3], Minghua Zhu[3], Jin Rao[3], Chao Liu[1,2]
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Low ON-Resistance Vertical GaN-on-GaN Trench MIS-FET With Small Temperature Dependence

Zaitian Han, Hao Zhang, Shibing Long, Shu Yang
School of Microelectronics, University of Science and Technology of China, Hefei, China

High-Gain/Low-Vf GaN Bipolar Junction Transistor based on Heterogeneous Integration Process for Bandgap Reference Application

Yukai Huang[1], Junfeng Yu[1], Junyan Zhu[1], Xiaodong Yang[1], Wenzhang Du[1], Jiao Liang[3], Ruihan Gao[1], Chunlei Wu[1], Hongping Ma[3], Qingchun Zhang[3], Jun Tang[4], Liang Li[5], Wei Huang[2], David Wei Zhang[1]
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[5]*School of Electronic Information Engineering, Suzhou Vocational Univerisity, Suzhou, China*

Wednesday, 4 June 2025

8:40 - 10:20 **4F Main Hall**

SiC-4: Gallium Oxide and Diamond Devices

Chairs: Peter Losee (*Qorvo, USA*) Hiroshi Kono (*Toshiba Electronic Devices & Storage, Japan*)

8:40 - 9:00 **3 kV/2.9 mΩ·cm² β-Ga_2O_3 Vertical p–n Heterojunction Diodes with Helium-implanted Edge Termination and Oxygen Post Annealing**

Jiajun Han[1,2], Na Sun[3], Xinyi Pei[3], Kangkai Fan[2], Yu Xu[2], Zihao Huang[2], Renqiang Zhu[5], Nengjie Huo[1], Jingbo Li[6], Junfa Mao[4], Jiandong Ye[3], Xinke Liu[2,4]

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[5]Shenzhen Institute for Advanced Study, University of Electronic Science and Technology of China, Shenzhen, China
[6]College of Optical Science and Engineering, Zhejiang University, Hangzhou, China

9:00 - 9:20 **3.9 kV Vertical β-Ga_2O_3 Hetero-Junction Diode With High-Temperature Operational Capability**

Jiangbin Wan[1], Hengyu Wang[1], Haoyuan Cheng[1], Chi Zhang[1], Ce Wang[1], Tiancheng Tao[1], Zijian Hu[1], Junze Li[1], Han Wang[1], Haoyu Wang[1], Haidong Yan[1,2], Na Ren[1,2], Qing Guo[1], Kuang Sheng[1,2]

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[2]ZJU-Hangzhou Global Scientific and Technological Innovation Center, Zhejiang University, Hangzhou, China

9:20 - 9:40 **Enhancing Continuous Switching Stability of β-Ga_2O_3 SBDs through Epitaxial Surface Condition and Edge Termination Optimizations**

Haoran Wang[1], Chi-Rui Hwang[1], Po-Yen Huang[2], Yeke Liu[1], Shawn S. H. Hsu[1,2], Roy K.-Y. Wong[1,2]

[1]Institute of Electronics Engineering, National Tsing Hua University, Hsinchu, Taiwan
[2]College of Semiconductor Research, National Tsing Hua University, Hsinchu, Taiwan

9:40 -10:00 **1844 V β-Ga_2O_3 Trench-MOS Schottky Barrier Diodes with Improved Electric Field of 5.2 MV/cm**

Akio Takatsuka[1], Hironobu Miyamoto[1], Tsunetoshi Maehara[2], Yosuke Fujiwara[2], Kohei Sasaki[1], Akito Kuramata[1]

[1]Novel Crystal Technology, Saitama, Japan; [2]Phenitec Semiconductor, Okayama, Japan

10:00 -10:20 **Over 1kV deep depletion diamond MOSFET**

Damien Michez[1,2], Juliette Letellier[2], Julien Pernot[3], Ralph Makhoul[2], Nicolas Rouger[2]

[1]DIAMFAB, Grenoble, France; [2]LAPLACE, Université de Toulouse, CNRS, INPT, Toulouse, France; [3]Institut Néel, Grenoble, France

10:20 -10:50 **3F A1/A2 Room and Foyer (Exhibition Area)**

Coffee Break

10:50 -12:30 **4F Main Hall**

SiC-2: Design Approaches and Physics for Reliability and Performance of SiC Devices

Chairs: Kung-Yen Lee (*National Taiwan University, Taiwan*) Shinsuke Harada (*AIST, Japan*)

10:50 -11:10 **Impact of Insulating Layer Design in the Termination Region of SiC Devices on H³TRB Test**

Kohei Ebihara, Hiroki Niwa, Yosuke Nakata, Toshikazu Tanioka, Takeshi Murakami, Katsuhiro Fujiyoshi, Shigeru Okimoto, Kenji Hatori, Katsutoshi Sugawara, Tatsuro Watahiki

Advanced Technology R&D Center, Mitsubishi Electric, Hyogo, Japan

11:10 -11:30 **1 cm² Chip Size, 10 kV Rated 4H-SiC MOSFETs with Efficient Termination Design and State-of-the-Art Device Performance**

Lingxu Kong[1,3], Sizhe Chen[2], Na Ren[1,3], Manyi Ji[1,3], Ce Wang[1], Yanjun Li[3], Hongyi Xu[3], Zheng Liu[1], Xiuyan Lin[4], Xueqian Zhong[2], Wei Chen[2,4], Haitao Huang[2], Yongxi Zhang[2,4], Kuang Sheng[1,3]

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[3]ZJU-Hangzhou Global Scientific and Technology Innovation Center, Hangzhou, China
[4]Zhejiang Inventchip Technology, Zhejiang, China

11:30 -11:50 **Plasma Behavior of SiC MOSFETs with Engineered Substrates during Reverse Recovery**

Mohamed Alaluss[1], Madhu Lakshman Mysore[1], Clemens Herrmann[1], Sudhanshu Goel[2], Ahmed Elsayed[2], Thomas Basler[1]

[1]Chair of Power Electronics, Chemnitz University of Technology, Chemnitz, Germany; [2]Robert Bosch GmbH, Reutlingen, Germany

11:50 -12:10 **Dead Time Dependency of Bipolar Degradation in SiC MOSFETs**

Clemens Herrmann[1], Mengdi He[1], Mohamed Alaluss[1], Rudolf Elpelt[2], Larissa Wehrhahn-Kilian[2], Thomas Basler[1]

[1]Chair of Power Electronics, Chemnitz University of Technology, Chemnitz, Germany; [2]Infineon Technologies AG, Erlangen, Germany

12:10 -12:30 **Investigation of Optimum Gate Structures for 1.2-kV SiC MOSFETs by Analyzing Avalanche and Short-Circuit Withstanding Capabilities**

Kazuhiro Suzuki, Hiroshi Yano, Noriyuki Iwamuro

Graduate School of Pure and Applied Sciences, University of Tsukuba, Tsukuba, Japan

12:30 -14:00 **2F Civic Hall**

Lunch Break

Wednesday, 4 June 2025

14:00 -15:40 4F Main Hall

PK: Packaging Technologies

Chairs: Xavier Jorda (*IMB-CNM, Spain*) Wei-Chung Lo (*Industrial Technology Research Institute, Taiwan*)

14:00 -14:20 **Low Loop Inductance in Power Semiconductor Module with Direct-Lead Bonding Busbar**
Jiyoon Choi[1] , Sihoon Choi[2], Jun Imaoka[2], Masayoshi Yamamoto[2]
[1]Department of Electrical Engineering, Nagoya University, Nagoya, Japan
[2]Institute of Materials and Systems for Sustainability (IMaSS), Nagoya University Nagoya, Japan

14:20 -14:40 **Packaging Technology and Evaluation Result of Ultra- Compact Double-Side Cooled Power Module**
Yoshihiro Tateishi, Akira Kitamura, Keita Suzuki, Satoharu Tanai, Tetsuo Endoh, Yoshikazu Takahashi
Center for Innovative Integrated Electronic Systems, Tohoku University, Sendai, Japan

14:40 -15:00 **SiC MOSFET Chip Embedded Switching-Cell for Multilevel Converters**
Mariana Raya[1], Emma Solà[1], Miquel Vellvehi[1], Xavier Perpiñà[1], Philippe Lasserre[2], Sergio Busquets-Monge[3], Xavier Jordà[1]
[1]Power Devices and Systems (PDS) Group, Institute of Microelectronics of Barcelona, IMB-CNM (CSIC), Barcelona, Spain
[2]Deep Concept, Pau, France; [3]Electronic Engineering Department, Polytechnic University of Catalonia (UPC), Barcelona, Spain

15:00 -15:20 **Impact of Cu Clip and Wire-Bonded Packaging on the Surge Current Capability of SiC MOSFETs in the Third Quadrant**
Feilin Zheng[1], Binqi Liang[1], Chao Zheng[2], Xuebao Li[1], Zhibin Zhao[1], Xiang Cui[1]
[1]State Key Laboratory of Alternate Electrical Power System with Renewable Energy Sources, North China Electric Power University, Beijing, China
[2]Beijing Institute of Smart Energy, Huairou Laboratory, Beijing, China

15:20 -15:40 **Stability Analysis based on a Virtual Twin of SiC Power MOSFET Module**
Ivana Kovacevic-Badstübner[1], Anja K. Brandl[1], Michel Nagel[1], Fernando Aguilar Vega[2], Bogdan Popescu[3], Dan Popescu[3], Ulrike Grossner[1]
[1]Advanced Power Semiconductor (APS) Laboratory, ETH Zurich, Zurich, Switzerland
[2]R&D, Ingeteam, Zamudio, Spain; [3]Infineon Technologies AG, Neubiberg, Germany

15:40 -16:00 **3F A1/A2 Room and Foyer (Exhibition Area)**

Coffee Break

16:00 -18:00 3F A3/A4 Room

HV-P: High Voltage Devices (Poster Session)

Extreme optimization of 1200V SuperJunction IGBT, competing with SiC MOSFET
Masahiro Tanaka[1], Naoki Abe[1], Akio Nakagawa[2]
[1]Nihon Synopsys G.K., Tokyo, Japan; [2]Nakagawa Consulting Office LLC., Chigasaki, Japan

Low EMI Noise Superjunction MOSFET with an Ndot region in the P-pillar
Ping Li[1], Rongyao Ma[1], Xin Zhang[1], Daili Wang[1], Kaifeng Tang[1], Wei Zeng[1], Wentong Zhang[2], Teng Liu[2]
[1]China Resources Microelectronics (Chongqing), Chongqing, China
[2]State Key Laboratory of Electronic, Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu, China

Improved short-circuit ruggedness in FS-IGBTs through optimized n+ emitter design
Kaname Mitsuzuka, Ryutaro Ishizaki, Tatsuya Naito, Yuichi Onozawa
Semiconductors Business Group, Fuji Electric, Matsumoto, Japan

Reduction of control delay in Single-back and Double-front Gate-controlled IGBT for high frequency applications
Takato Yamamoto[1], Yusuke Kobayashi[1], Munetoshi Fukui[2], Tomoko Matsudai[3], Ryohei Gejo[3], Takuya Saraya[2], Kazuo Itou[2], Toshihiko Takakura[2], Shinichi Suzuki[2], Teruyuki Ohashi[1], Tatsunori Sakano[1], Tomoaki Inokuchi[1], Toshiro Hiramoto[2]
[1]Corporate Research & Development Center, Toshiba, Kanagawa, Japan; [2]Institute of Industrial Science, The University of Tokyo, Tokyo, Japan
[3]Advanced Semiconductor Device Development Center, Toshiba Electronic Devices & Storage, Kanagawa, Japan

The Electrical Impact of Oxygen and Carbon Related Defect Profile in Electron Beam Irradiated MCZ/FZ Wafers
Kodai Ozawa, Sho Nakanishi, Hiroshi Inagawa
Power Device Technology Department, Renesas Electronics, Ibaraki, Japan

A Superjunction MOSFET with Self-adjustable Electron Path for Low Reverse Recovery Charge
Tongyang Wang[1], Zehong Li[1,2], Ziming Xia[1], Yige Zheng[1], Jingcheng Feng[1]
[1]State Key Laboratory of Electronic, Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu, China
[2]Chongqing Institute of Microelectronics Industry Technology, University of Electronic Science and Technology of China, Chongqing, China

Fabrication and Optimization of 1550 V Semi-Superjunction MOSFET with Ultra-low Specific On-Resistance and Enhanced Switching Performance
Guoliang Yao[1], Ming Qiao[1,2], Bo Zhang[1]
[1]State Key Laboratory of Electronic, Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu, China
[2]Shenzhen Institute for Advanced Study, University of Electronic Science and Technology of China, Shenzhen, China

Thermal Analysis of Current Crowding in IGBTs under Stressful Operation in Resonant Converters
Conrad Ferrer[1], Miquel Vellvehi[1], Xavier Jordà[1], Manuel Fernández[2], Sergio Llorente[2], Xavier Perpiñà[1]
[1]Power Devices and Systems (PDS) Group, Institute of Microelectronics of Barcelona, IMB-CNM (CSIC), Barcelona, Spain
[2]BSH Home Appliances Group, Zaragoza, Spain

Intelligent Design of Superjunction Devices Based on Physics-informed Neural Network

Jing Chen[1,3], Huiyuan Li[1,3], Haiwei Tan[1,3], Zhekai Hu[2], Jiafei Yao[1,3], Ziwei Hu[1,3], Ping Li[4], Rongyao Ma[4], Wentong Zhang[1,2], Bo Zhang[2], Yufeng Guo[1,3]
[1]*College of Integrated Circuit Science and Engineering, Nanjing University of Posts and Telecommunications, Nanjing, China*
[2]*University of Electronic Science and Technology, Chengdu, China.*
[3]*National & Local Joint Engineering Laboratory for RF Integration and Micro-Packaging Technologies, Nanjing, China*
[4]*China Resources Microelectronics, Chongqing, China*

An improved TCAD simulation procedure for platinum-diffused silicon power diodes

Calvin Stephen[1,2], Sophie Ngo[1], Greca Jean-Charles[1], Luong Viêt Phung[2], Christophe Raynaud[2], Dominique Planson[2]
[1]*STMicroelectronics, Discrete & Filter Division, Tours, France*
[2]*Univ Lyon, INSA Lyon, Université Claude Bernard Lyon 1, Ecole Centrale de Lyon, CNRS, Ampère, Villeurbanne, France*

16:00 -18:00 3F A3/A4 Room

PK-P: Packaging Technologies 2 (Poster Session)

Thermal Management by Using Small-area Chips and AI-based Design Optimization in SiC Modules

Teruyuki Ohashi[1], Shun Takeda[2], Eitaro Miyake[2], Hiroshi Kono[3], Tomohiro Iguchi[4], Kazuya Kodani[5], He Du[1], Yasunori Taguchi[1], Mitsuhiro Kimura[1], Hideyuki Nakagawa[1], Ryosuke Iijima[1]
[1]*Corporate Research & Development Center, Toshiba, Kawasaki, Japan*
[2]*Package & Test Technology Development Center, Toshiba Electronic Devices & Storage, Japan*
[3]*Advanced Semiconductor Device Development Center, Toshiba Electronic Devices & Storage, Japan*
[4]*Corporate Manufacturing Engineering Center, Toshiba, Japan*
[5]*Infrastructure Systems Research and Development Center, Toshiba Infrastructure Systems & Solutions, Japan*

A Novel High-Performance Double-Sided Cooling SiC Power Module Based on Cu Sintering

Haobin Chen[1], Haidong Yan[1,2], Kuang Sheng[1,2]
[1]*College of Electrical Engineering, Zhejiang University, Hangzhou, China*
[2]*Global Scientific and Technology Innovation Center, Zhejiang University, Hangzhou, China*

Source Current Circulation Phenomenon and Suppression Method of High Voltage SiC Devices

Xinling Tang , Jingfei Wang, Xiaoguang Wei, Yaohua Wang, Jingzhi Chen, Yujie Du, Liang Wang, Hao Zhang
Beijing Huairou laboratory, Beijing, China

Non-Intrusive Online Junction Temperature Monitoring in Si and SiC Power MOSFETs

Miquel Tutusaus[1], Xavier Perpiñà[1], Miquel Vellvehi[1], Manuel Fernández[2], Sergio Llorente[2], Xavier Jordà[1]
[1]*Power Devices and Systems (PDS) Group, Institute of Microelectronics of Barcelona, IMB-CNM (CSIC), Barcelona, Spain*
[2]*BSH Home Appliances Group, Zaragoza, Spain*

Chip-level Interconnection Techniques for Chip Embedding Integration of SiC MOSFETs

Emma Solà[1], Mariana Raya[1], Philippe Lasserre[2], David Sánchez[1], José Rebollo[1], Miquel Vellvehi[1], Xavier Perpiñà[1], Xavier Jordà[1]
[1]*Power Devices and Systems (PDS) Group, Institute of Microelectronics of Barcelona, IMB-CNM (CSIC), Barcelona, Spain;* [2]*Deep Concept, Pau, France*

A Novel Lifetime Prediction Method for Press Pack Devices Based on Fretting Wear

Xiaoguang Wei, Xinling Tang, Jianhui Liu, Jingfei Wang, Kefan Yu, Yujie Du
Beijing Huairou laboratory, Beijing, China

A GaN Power Module Using a Copper PCB with Integrated Liquid-Cooled Heat Exchanger

Jingyuan Liang[1], Xuan Wang[1], Xiaoyun Zhang[1], Chun Yin Au Yeung[1], Andrei Catuneanu[2], Matthew Birkett[2], Wai Tung Ng[1]
[1]*The Edward S. Rogers Sr. Department of Electrical and Computer Engineering, University of Toronto, Toronto, Ontario, Canada*
[2]*Dana Canada, Advanced Technology and Research, Oakville, Ontario, Canada*

16:00 -18:00 3F A3/A4 Room

SiC-P1: SiC Devices (Poster Session)

Study on Differences in Single-Event Leakage Current of Planar-Gate and Asymmetric Trench-Gate SiC MOSFETs

Xiaoping Dong[1,2], Mingmin Huang[1,2], Yao Ma[1,2], Zhimei Yang[1,2], Yun Li[1,2], Min Gong[1,2]
[1]*College of Physics, Sichuan University, Chengdu, China*
[2]*Key Laboratory of Radiation Physics and Technology, Ministry of Education, Sichuan University, Chengdu, China*

Impact of Bulk Defects on Reliability and Noise in 1200V SiC DMOSFETs

Huamao Chen[1], Yu-Ting Chen[2], Shih-Chiang Shen[1], Chih-Hung Yen[1], Ju-Cheng Lin[1], Chih-Ming Lai[1]
[1]*Electronic and Optoelectronic System Research Laboratories, Industrial Technology Research Institute, Hsinchu, Taiwan*
[2]*Electrical Measurement Laboratories, Taiwan Semiconductor Research Institute, Hsinchu, Taiwan*

Short Circuit Protection of Parallel SiC MOSFET Modules Based on Electro-thermal Design with High-Temperature I-V Characteristics

Makiko Hirano, Kazuya Kodani, Akihisa Matsushita, Atsuhiko Kuzumaki
Corporate Research and Development Center, Toshiba, Tokyo, Japan

Study of a novel hybrid design with an IGBT and a SiC-MOSFET in a fast-switching ANPC topology

Alexander Philippou, Thorsten Arnold, Martin Weidl, Max Falkowski, Franz-Josef Niedernostheide
Infineon Technologies AG, Neubiberg, Germany

Analysis on BV_{DSS} Outlier Chips and Screening Technology for 1.2 kV Automotive SiC MOSFETs

Jinying Yu, Jingjing Cui, Bao Hu, Jie Deng, Baocheng Yuan
Li Auto, Beijing, China

Influence of substrate and epi buffer on SiC bipolar degradation for different voltage classes at high current levels

Larissa Wehrhahn-Kilian[1], Paul Salmen[2], Michael Brambach[1]
[1]*Infineon Technologies AG, Erlangen, Germany;* [2]*Infineon Technologies AG, Warstein, Germany*

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Impact of the SiC MOSFET Body Diode in Heavy Ion-Induced Single-Event Damage

Leshan Qiu[1,2], Yun Bai[1], Jiale Wang[1,2], Yan Chen[1,2], Jieqin Ding[3], Chengzhan Li[3], Xinyu Liu[1]
[1]Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China
[2]School of Integrated Circuits, University of Chinese Academy of Sciences, Beijing, China; [3]Zhuzhou CRRC Times Semiconductor, Zhuzhou, China

A Physics-Based Fast Electro-Thermal Coupling Model for Wide-Temperature-Range Junction Temperature Assessment in SiC MOSFETs

Cheng Zhang[1,2], Wenyu Lu[1,2], Xuetong Zhou[1,2], Xinhong Cheng[1,2], Li Zheng[1,2]
[1]The State Key Laboratory of Materials for Integrated Circuits, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences
[2]The Center of Materials Science and Optoelectronics Engineering, University of Chinese Academy of Sciences, Beijing, China

An analysis of UIS failure mechanism of 4H-SiC MOSFET in transition region

Chen Yan[1,2], Bai Yun[1], Li Chengzhan[3], Wang Antao[1,2], Qiu Leshan[1,2], Tian Xiaoli[1], Tang Yidan[1], Wang Xinhua[1], Liu Xinyu[1]
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[3]Zhuzhou CRRC Times Semiconductor, Zhuzhou, China

Outperformance of Asymmetric 4H-SiC Superjunction Geometry Beyond the Optimal Limit of Symmetric Design

Daisuke Iizasa, Hiroaki Shiraga, Seigo Mori, Yuki Nakano
Silicon Carbide Advanced Devices Development Division, ROHM, Kyoto, Japan

Impact of V_{TH} instability in SiC for solid-state circuit breaker application

Enea Bianda[1], Gioele Gregis[2], Elena Mengotti[1], Gerd Schlottig[1], Luca Raciti[2], Thomas Masper[2]
[1]ABB Corporate Research Center, Baden-Dättwil, Switzerland; [2]ABB SpA, Bergamo, Italy

Measurement of Free-Carrier Density in a 1.2 kV SiC Schottky Diode under Overstress Conditions

Ferran Bonet, Oriol Aviñó, Xavier Jordà, Xavier Perpiñá
Power Devices and Systems (PDS) Group, Institute of Microelectronics of Barcelona, IMB-CNM (CSIC), Barcelona, Spain

Demonstration of 1100 V 600 A/cm² 4H-SiC Lateral IGBT with Field Limiting Rings Termination Design

Mengyao Zhao[1], Jie Ma[1], Tianchun Nie[1], Qiwei Peng[1], Haowei Chen[2], Runhua Huang[2], Yu Huang[2], Song Bai[2], Jiaxing Wei[1], Siyang Liu[1], Long Zhang[1], Weifeng Sun[1]
[1]School of Integrated Circuits, Southeast University, Nanjing, China; [2]Nanjing Electronic Devices Institute, Nanjing, China

A Study on Fault Prediction and Redundancy Control of Parallel SiC-MOSFETs

Naoki Takagi[1], Akira Tamakoshi[2], Takahiro Hanyu[2], Yoshitaka Iwaji[3], Tetsuo Endoh[1], Yoshikazu Takahashi[1]
[1]Center for Innovative Integrated Electronic Systems, Tohoku University, Sendai, Japan
[2]Laboratory for Brainware Systems, Research Institute of Electrical Communication, Tohoku University, Sendai, Japan
[3]Department of Electrical and Electronic Engineering, Ibaraki University, Ibaraki, Japan

Dynamic Transconductance Extraction Method and Application in Medium-Voltage SiC Module

Jie Ren[1], Menghao Li[1], Sideng Hu[1], Naoto Fujishima[2], Haruhiko Nishio[2]
[1]College of Electrical Engineering, Zhejiang University, Hangzhou, China
[2]Semiconductors Business Group, Fuji Electric, Matsumoto, Japan

Negative Gate Bias Induced V_{th} instability in SiC MOSFET: Role of Body Diode Conduction

Peixuan Wang[1,2], Yunhong Lao[1], Meng Zhang[2], Youyi Yin[1], Hao Chang[1], Hengyuan Qi[1,2], Michael Lee[3], Jack Chen[3], Tony Chau[3], Jin Wei[1]
[1]School of Integrated Circuits, Peking University, Beijing, China; [2]College of Microelectronics, Beijing University of Technology, Beijing, China
[3]Alpha Power Solutions, Shanghai, China

The Latest Fabrication and Experimental Results of 1.2 kV Split-Gate 4H-SiC MOSFET with P+ Buffer

Yuzhi Chen, Chi Li, Zedong Zheng
Department of Electrical Engineering, Tsinghua University, Beijing, China

Monolithic Integration of Lateral 4H-SiC MOSFET and Insulated-Gate Resistive Load with Improved Linearity and High-Temperature Stability

Cheng Sung[1], Pin-Shiuan Kuo[2], Yu-Sheng Hsiao[1], Wei-Cheng Lin[2], Surya Elangovan[3], Chia-Lung Hung[3], Yi-Kai Hsiao[3], Hao-Chung Kuo[1,3,5], Chang-Ching Tu[3,4], Tian-Li Wu[1,2,6]
[1]Institute of Pioneer Semiconductor Innovation, National Yang Ming Chiao Tung University, Taiwan
[2]International College of Semiconductor Technology, National Yang Ming Chiao Tung University, Taiwan
[3]Semiconductor Research Center, Hon Hai Research Institute, Taiwan; [4]Department of Electrical Engineering, National Central University, Taiwan
[5]Department of Photonics, National Yang Ming Chiao Tung University, Taiwan
[6]Institute of Electronics and Department of Electronics and Electrical Engineering, National Yang Ming Chiao Tung University, Taiwan

Investigation of Termination Soft Breakdown Mechanisms in 1700V-SiC MOSFETs Under HTRB with Different Temperatures

Wei-Chieh Hung[1], Hung-Ming Kuo[1], Ting-Chang Chang[1,2], Po-Yu Yen[1], Chun-Hung Chiang[2], Bo-Yu Chen[1]
[1]Department of Physics, National Sun Yat-sen University, Kaohsiung, Taiwan
[2]College of Semiconductor and Advanced Technology Research, National Sun Yat-sen University, Kaohsiung, Taiwan

Application-relevant Measurement of the Input Capacitance of SiC Power MOSFETs

Michel Nagel, Anja K. Brandl, Manuel Belanche, Ivana Kovacevic-Badstübner, Ulrike Grossner
Advanced Power Semiconductor (APS) Laboratory, ETH Zurich, Zurich, Switzerland

Effects of Proton Irradiation on SiC Power Devices with Various Edge Termination Structures

Sangyeob Kim[1], Jeongtae Kim[2,4], Dong-Seok Kim[2], Hyuncheol Bae[3], Gyuhyeok Kang[4], Ogyun Seok[1]
[1]School of Electrical and Electronic Engineering, Pusan National University, Busan, Korea; [2]Korea Atomic Energy Research Institute, Gyeongju, Korea
[3]Electronics and Telecommunications Research Institute, Daejeon, Korea
[4]Department of Semiconductor System Engineering, Kumoh National Institute of Technology, Gumi, Korea

Data-Driven Multi-Objective Optimization of SiC Power MOSFETs

Anja K. Brandl[1], Ivana Kovacevic-Badstübner[1], Bhagyalakshmi Kakarla[1], Roland Niemeier[2], Ulrike Grossner[1]
[1]Advanced Power Semiconductor Laboratory (APS), ETH Zurich, Zurich, Switzerland
[2]Ansys Germany GmbH, Weimar, Germany

Reliability Testing of SiC MOSFETs in Different Power Cycling Operating Modes - Focusing on the Challenges of Body Diode Testing
Lukas Hein, Patrick Heimler, Georg Schubert, Josef Lutz, Thomas Basler
Chair of Power Electronics, Chemnitz University of Technology, Chemnitz, Germany

An In-Depth Investigation of Gate Ringing Induced by Total Ionizing Dose in SiC MOSFETs
Jiahao Hu, Xiaochuan Deng, Yinglun Wang, Tao Xu, Xuan Li, Bo Zhang
School of Integrated Circuit Science and Engineering, University of Electronic Science and Technology of China, Chengdu, China

Optimisation of the Fabrication of Sidewall-Implanted Trenches in a 3.3 kV SiC Semi-Superjunction Schottky Barrier Diode
Arne Benjamin Renz[1], Kyrylo Melnyk[1], Nikolaos Iosifidis[1], Richard Jefferies[1], Marco Zignale[2], Patrick Fiorenza[2], Luca Maresca[3], Andrea Irace[3], Fabrizio Roccaforte[2], Neophytos Lophitis[4], Peter Michael Gammon[1], Marina Antoniou[1]
[1]School of Engineering, University of Warwick Coventry, UK; [2]Istituto per la Microelettronica e Microsistemi – IMM-CNR Catania, Italy
[3]Department of Electrical Engineering and Information Technologies, University of Naples Federico II, Naples, Italy
[4]Faculty of Engineering and Technology, Cyprus University of Technology, Limassol, Cyprus

Novel 1.2kV 4H-SiC deep p-well one-channel MOSFET with asymmetric channel design
Skylar deBoera[1], Seung Yup Jang[1,2], Adam Morgan[2], Woongje Sung[1]
[1]College of Nanotechnology Science and Engineering, University at Albany, Albany, NY, USA; [2]NoMIS Power, Albany, NY, USA

Comparative Analysis Between Monolithically Integrated 1.2kV Bi-Directional MOSFETs and Bi-Directional JBSFETs
Stephen A. Mancini[1], Daixin Chen[2], Seung Yup Jang[1], Andrew Binder[3], Richard Floyd[3], Robert Kaplar[3], Jack Flicker[3], Stan Atcitty[3], Justin Lynch[1], Adam J. Morgan[4], Xiaoqing Song[2], Woongje Sung[1]
[1]University at Albany, College of Nanotechnology Science and Engineering, Albany, NY, USA
[2]University of Arkansas, Department of Electrical Engineering and Computer Science, Fayetteville, AR, USA
[3]Sandia National Laboratories, Albuquerque, NM, USA; [4]NoMIS Power, Albany, NY, USA

Comparative Performance Evaluation and Analysis of High Voltage Superjunction, Charge-Balanced, and Conventional 4H-SiC DMOSFETs at Cryogenic and High Temperatures
Zhaowen He[1], Reza Ghandi[2], Collin W. Hitchcock[2], Stacey Kennerly[2], T. Paul Chow[1]
[1]Rensselaer Polytechnic Institute, Troy, New York, USA; [2]GE Aerospace, Niskayuna, New York, USA

Investigations on SiC LIGBT with Floating Field-Limiting Rings and Injection Enhancement Effect
Moufu Kong[1], Hongfei Deng[1], Mingliang Yang[1], Yingzhi Luo[1], Zhaoyu Ai[1], Bingke Zhang[2]
[1]State Key Laboratory of Electronic, Thin Films and Integrated Devices of China, University of Electronic Science and Technology of China, Chengdu, China
[2]Power Device Research and Development Centre, Leshan Share Electronic, Leshan, China

Capacitance Degradation of SiC MOSFETs under Dynamic Reverse Bias Stress: Displacement Current-Induced Charge Injection and JFET Design Optimization
Zhaoxiang Wei, Zhaokuan Liu, Guozhi Zhen, Junhou Cao, Hao Fu, Jiaxing Wei, Siyang Liu, Weifeng Sun
National ASIC System Engineering Research Center, School of Integrated Circuits, Southeast University, Nanjing, China

16:00 -18:00 3F A3/A4 Room

SiC-P2: Gallium Oxide Devices (Poster Session)

Enhancing the Performance and Reliability of Large-Area β-Ga_2O_3 Schottky Barrier Diodes via Two-Step Oxygen Annealing
Jinyang Liu, Yuanjie Ding, Qiuyan Li, Shu Yang, Zheyang Zheng, Guangwei Xu, Shibing Long
University of Science and Technology of China, Hefei, China

Kilovolt-Class β-Ga_2O_3 Multi-Fin-Channel Diodes with Ohmic-Contact Anode
Gaofu Guo[1,2], Xiaodong Zhang[1], Chunhong Zeng[1], Tiwei Chen[1], Dengrue Zhao[1,2], Zhili Zou[1], Zhucheng Li[1], Li Zhang[1], Zhongming Zeng[1], Xianqi Dai[2], Baoshun Zhang[1]
[1]Nanofabrication facility, Suzhou Institute of Nano-Tech and Nano-Bionics, Chinese Academy of Sciences (CAS), Suzhou, Jiangsu, China
[2]School of Physics, Henan Normal University, Xinxiang, Henan, China

Investigation of β-Ga_2O_3 Power Diodes with Failure Voltage of 300 V under LET of 82 MeV·cm²/mg
Song He[1], Jinyang Liu[1], Guangwei Xu[1], Weibing Hao[1], Tianqi Wang[2], Xuanze Zhou[1], Shu Yang[1], Shibing Long[1]
[1]University of Science and Technology of China, Hefei, China; [2]Harbin Institute of Technology, Harbin, China

Over 3 kV Vertical Mo/β-Ga_2O_3 Trench-HJBS Diode with Low Turn-on Voltage of 0.66 V
Qiuyan Li, Jinyang Liu, Zhao Han, Weibing Hao, Guangwei Xu, Shibing Long
University of Science and Technology of China, Hefei, China

Monolithic Integrated β-Ga_2O_3 Inverters Based on Charge Trapping Layer E-mode MOSFETs
Mujun Li[1], Xiaohui Wang[1], Yang Jiang[1,2], Fangzhou Du[1], Haozhe Yu[1], Qing Wang[1], Hongyu Yu[1,3]
[1]School of Microelectronics, Southern University of Science and Technology, Shenzhen, China
[2]Department of Electrical and Electronic Engineering, The University of Hong Kong, Pokfulam Road, Hong Kong
[3]School of integrated Circuit, Shenzhen Polytechnic University, Shenzhen, China

Degradation Mechanisms of β-Ga_2O_3 SBD Associated with Proton Irradiation-Induced Defects
Wenzhang Du[1], Yuangang Wang[7], Junfeng Yu[1], Junyan Zhu[1], Xinbo Zou[3], Liang Li[4], Debin Zhang[5], Yiwu Qiu[6], Xinjie Zhou[6], Tao Wang[6], Zhihong Feng[7], Hongping Ma[8], Qingchun Zhang[8], Wei Huang[2], Chunlei Wu[1], David Wei Zhang[1]
[1]Shanghai Institute of Intelligent Electronics & Systems, School of Microelectronics, Fudan University, Shanghai, China
[2]School of Integrated Circuits, Jiangnan University, Wuxi, China; [3]School of Information Science and Technology (SIST), ShanghaiTech University, Shanghai, China
[4]School of Electronic Information Engineering, Suzhou Vocational University, Suzhou, China
[5]Shanghai Institute of Space Power-Sources, Shanghai, China; [6]Wuxi Microelectronics Scientific and Research Center, Wuxi, China
[7]National Key Laboratory of Solid-State Microwave Devices and Circuits, Shijiazhuang, Hebei, China
[8]School of Academy for Engineering & Technology, Fudan University, Shanghai, China

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Comparative Study on Transient Thermal Resistance for β-Ga_2O_3 SBDs with Junction-Side Cooling Implementation
Shuhei Fukunaga[1], Tsuyoshi Funaki[1], Jun Arima[2], Minoru Fujita[2], Jun Hirabayashi[2]
[1]Graduate school of Engineering, Osaka University, Osaka, Japan
[2]Advanced Products Development Center Technology & IP HQ, TDK, Chiba, Japan

Self-Aligned Gate Technology for N-Ion-Implanted β-Ga_2O_3 UMOSFET
Xuanze Zhou, Qi Liu, Guangwei Xu, Shibing Long
University of Science and Technology of China, Hefei, China

High-Voltage Ga_2O_3 Vertical Schottky Barrier Diode With Suspended Field Plate Assisted Shallow Mesa Termination
Desen Chen[1], Xiaorui Xu[1], Yicong Deng[1], Xueli Han[2], Zhengbo Wang[2], Duanyang Chen[2], Hongji Qi[2], Xiaoqiang Lu[1], Haizhong Zhang[1]
[1]College of Physics and Information Engineering, Fuzhou University, Fuzhou, China
[2]Key Laboratory of Materials for High Power Laser, Shanghai Institute of Optics and Fine Mechanics, Chinese Academy of Sciences, Shanghai, China

Investigation of Oxygen Vacancies and Reverse Leakage Suppression in High-Breakdown Vertical Ga_2O_3/4H-SiC Schottky Rectifiers
Ji-Hyun Kim, Soo-Young Moon, Geon-Hee Lee, Tae-Hee Lee, Seung-Hyun Park, Sang-Mo Koo
Department of Electronic Materials Engineering, Kwangwoon University, Seoul, Korea

Switching Reliability of NiO/Ga_2O_3 Bipolar Junction Evaluated by a Circuit Method
Hehe Gong[1], Xin Yang[1], Zineng Yang[1], Yuan Qin[2], Jiandong Ye[3], Yuhao Zhang[1]
[1]Department of Electrical and Electronic Engineering, The University of Hong Kong, Hong Kong, China
[2]Center for Power Electronics Systems (CPES), Virginia Tech, Blacksburg, USA; [3]School of Electronic Science and Engineering, Nanjing University, Nanjing, China

Monolithic Integration of Enhancement- and Depletion-mode MOSFETs Based on Heteroepitaxial ε-Ga_2O_3 for Power ICs
Shengheng Zhu, Linxuan Li, Tiecheng Luo, Weiqu Chen, Chenhong Huang, Xifu Chen, Zimin Chen, Yanli Pei, Gang Wang, Xing Lu
State Key Laboratory of Optoelectronic Materials and Technologies, School of Electronics and Information Technology, Sun Yat-sen University, Guangzhou, China

Reliability of β-Ga_2O_3 Schottky Barrier Diodes with a High Breakdown Voltage of 2.97 kV at 473 K
Guangwei Xu, Weibing Hao, Shibing Long
University of Science and Technology of China, Hefei, China

19:00 -21:30 **Hotel Nikko Kumamoto**
Banquet

Thursday, 5 June 2025

8:40 - 10:20 **4F Main Hall**

HV-2: Multi-Gate Technology and SJ Devices

Chairs: Ayanori Gatto (*Mitsubishi Electric, Japan*) Craig Fisher (*Vishay, UK*)

8:40 - 9:00 **A New Dimension of Hybrid Switches: Dual-gate IGBT and SiC MOSFET With Coordinated Gate Control**
Roman Baburske, Alexander Philippou
Infineon Technologies AG, Neubiberg, Germany

9:00 - 9:20 **Negative Gate Capacitance-Free Split-Gate-Resistance-Separation CSTBT™ for Ultra-Low Switching Loss**
Kazuya Konishi, Koyo Matsuzaki, Kohei Onda, Kohei Sako, Shinya Soneda
Advanced Technology R&D Center, Mitsubishi Electric, Hyogo, Japan

9:20 - 9:40 **Carrier-extraction Mechanism for MOS-controllable Stored-carrier Diode (MOSD)**
Hiroshi Suzuki[1], Yujiro Takeuchi[1], Yusuke Takada[1], Takashi Hirao[1], Tsubasa Moritsuka[2], Masaki Shiraishi[2], Tetsuo Oda[2], Tomoyasu Furukawa[2]
[1]Research & Development Group, Hitachi, Ibaraki, Japan; [2]Minebea Power Semiconductor Device, Ibaraki, Japan

9:40 -10:00 **Next-Generation Superjunction Power Device with Trench Sidewall Doping**
Chia Liang Liao[1,3], Lucio Renna[2], Voon Cheng Ngwan[1], Clelia Galati[2], Natalia Spinella[2], Giuseppe Longo[2], Francesco Patane[2], Gianfranco Di-Stefano[1], Jian Xin Zheng[3], Ning Xiang[3]
[1]STMicroelectronics, AMK, Singapore; [2]STMicroelectronics, Catania, Italy; [3]Singapore Institute of Technology, Singapore

10:00 -10:20 **Switching Loss Reduction in Superjunction IGBTs via Analysis of Vertical Charge Imbalance**
Tomohiro Tamaki[1], Atsufumi Inoue[1], Shiro Hino[1], Kazuyasu Nishikawa[1], Makoto Hashimoto[2], Mitsuhisa Kawase[2], Yohei Sudo[2], Tsutomu Ogawa[2], Tatsuro Watahiki[1]
[1]Advanced Technology R&D Center, Mitsubishi Electric, Hyogo, Japan; [2]Nisshinbo Micro Devices, Japan

10:20 -10:50 **3F A1/A2 Room and Foyer (Exhibition Area)**
Coffee Break

10:50 -12:30 **4F Main Hall**

SiC-3: Novel Devices and Ruggedness of SiC

Chairs: Cheng-Tyng Yen (*Fast SiC Semiconductor, Taiwan*) Takaaki Tominaga (*Mitsubishi Electric, Japan*)

10:50 -11:10 **First Demonstration of SiC MOSFET with Monolithically Integrated Short-Circuit Protection**
Shinichi Kimoto[1], Tatsunori Sakano[2], Ryosuke Iijima[2], Mitsuo Okamoto[1]
[1]Advanced Power Electronics Research Center, National Institute of Advanced Industrial Science and Technology, Tsukuba, Japan
[2]Corporate Research & Development Center, Toshiba, Kanagawa, Japan

11:10 -11:30 **Monolithic SiC Smart Power IC with Over-Temperature Protection**
Mitsuo Okamoto, Atsushi Yao, Hiroshi Sato
Advanced Power Electronics Research Center, National Institute of Advanced Industrial Science and Technology, Tsukuba, Japan

11:30 -11:50 **Experimental Demonstration and Analysis of 4.5kV Bidirectional Superjunction Power DMOSFETs in 4H-SiC**
Zhaowen He[1], Reza Ghandi[2], Collin W. Hitchcock[2], Stacey Kennerly[2], T. Paul Chow[1]
[1]Rensselaer Polytechnic Institute, New York, USA; [2]GE Aerospace, New York, USA

11:50 -12:10 **Impact of bottom p-well grounding resistance on unclamped inductive switching ruggedness of SiC trench MOSFETs**
Katsuhisa Tanaka[1], Yuji Kusumoto[1], Hideyuki Hasegawa[1], Hiroshi Kono[1], Kenya Sano[2]
[1]Advanced Semiconductor Device Development Center, Toshiba Electronic Devices & Storage, Hyogo, Japan
[2]Semiconductor Division, Toshiba Electronic Devices & Storage, Hyogo, Japan

12:10 -12:30 **The Accurate AC BTI Prediction of SiC Power MOSFETs by Comprehensive Understanding of Physical Mechanism Basic Vth Instability Phenomena**
Tetsuya Yoshida[1], Katsumi Eikyu[1], Keiichi Maekawa[1], Hideki Aono[1], Tsunenobu Kimoto[2]
[1]Renesas Electronics, Ibaraki, Japan
[2]Department of Electronic Science and Engineering, Kyoto University, Kyoto, Japan

12:30 -14:00 **2F Civic Hall**
Lunch Break

Thursday, 5 June 2025

14:00 -15:20 **4F Main Hall**

GaN-3: Novel GaN Power Device and Technologies 2

Chairs: Dong Seup Lee (*Texas Instruments, USA*) Hiroyuki Handa (*Panasonic Holdings, Japan*)

14:00 -14:20 **A Hybrid-Source Double-Channel p-GaN Gate AlGaN/GaN HEMT Featuring Suppression of Buffer Trapping Effects on Both Forward and Reverse Conductions**

Xiaotian Tang[1,2], Zhongchen Ji[1,2], Qimeng Jiang[1,2], Sen Huang[1,2], Xinguo Gao[1], Ke Wei[1,2], Xinhua Wang[1,2], Xinyu Liu[1,2]

[1]Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, China

[2]University of Chinese Academy of Sciences, Beijing, China

14:20 -14:40 **p-GaN Gate HEMT with the Buffer Hole Compensation Layer for Achieving Repetitive Avalanche-like Breakdown Capability**

Cheng Yu[1], Wanjun Chen[1], Fangzhou Wang[2], Zhuocheng Wang[1], Xiaochuan Deng[1], Guojian Ding[2], Zheyu Huang[1], Yang Wang[2], Haiqiang Jia[2,3], Hong Chen[3], Bo Zhang[1]

[1]State Key Laboratory of Electronic, Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu, China

[2]Songshan Lake Materials Laboratory, Dongguan, China; [3]Institute of Physics, China Academy of Sciences, Beijing, China

14:40 -15:00 **Vth Adjustable p-Channel GaN FinFET For Complementary Logic Integration**

Maolin Pan[1], Hai Huang[1], Xin Hu[1], Yifei Zhao[1], Yannan Yang[1], Saisheng Xu[1], Min Xu[1,2]

[1]State Key Laboratory of ASIC and System, Shanghai Institute of Intelligent Electronics & Systems, School of Microelectronics, Fudan University, Shanghai, China

[2]Shanghai Integrated Circuit Manufacturing Innovation Center, Shanghai, China

15:00 -15:20 **GaN/SiC-based Polarization Superjunction Hybrid HEMTs (PSJ-hyHEMTs) on Vicinal Off-angle SiC**

Akira Nakajima, Hirohisa Hirai, Yoshinao Miura, Kazutoshi Kojima, Tomohisa Kato, Shinsuke Harada

Advanced Power Electronics Research Center, National Institute of Advanced Industrial Science and Technology, Tsukuba, Japan

15:20 -15:50 **4F Main Hall**

Closing Session

Charitat Award and Best Poster Award

Ichiro Omura, General Chair

Yuichi Onozawa, Technical Program Committee Chair

Closing Remarks

Ichiro Omura, General Chair

ISPSD 2026 Announcement

David Sheridan, General Chair of ISPSD 2026 (*Alpha & Omega Semiconductor, USA*)

Sameh Khalil, Technical Program Committee Chair of ISPSD 2026 (*Infineon Technologies, USA*)