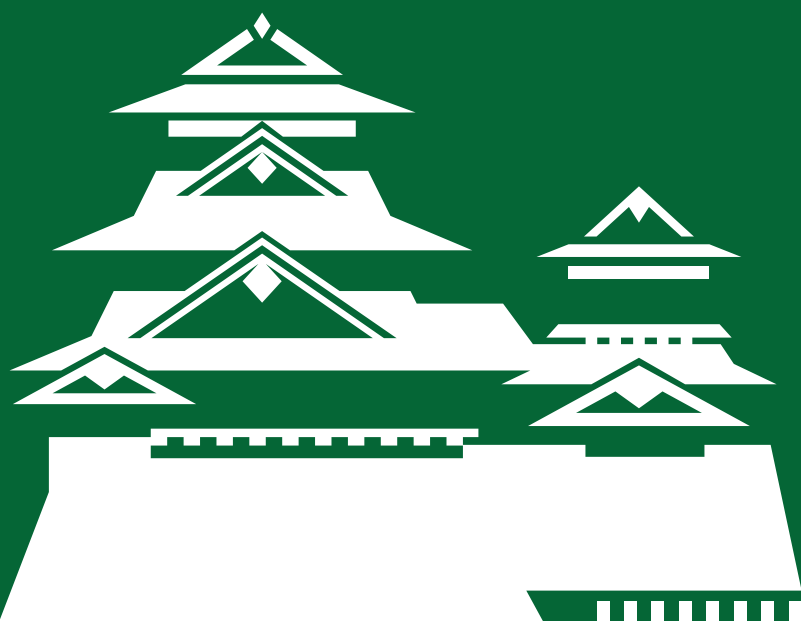


ISPSD 2025 KUMAMOTO

37th International Symposium on
Power Semiconductor Devices and ICs



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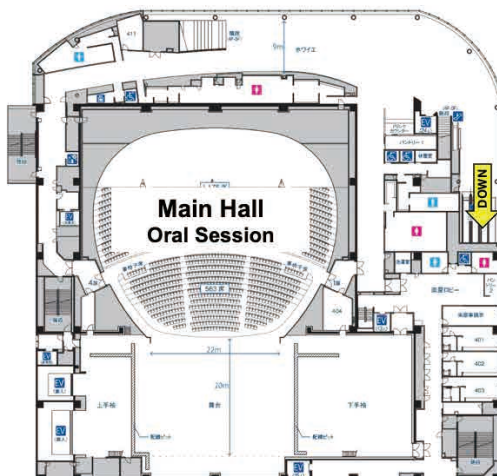
This conference is supported
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by International Exchange
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KUMAMOTO-JO (CASTLE) HALL FLOOR DIRECTRY

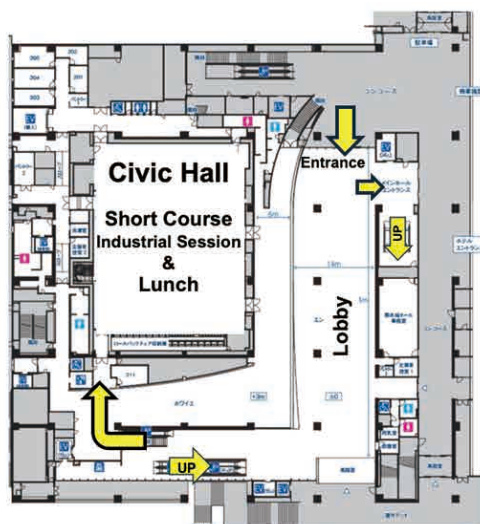
4th Floor



3rd Floor



2nd Floor



SCHEDULE AT A GLANCE

Time	June 1 Sun	June 2 Mon	June 3 Tue	June 4 Wed	June 5 Thu
8:30	Short Course Opening	8:30 - 9:00 Opening Session			
9:00	Short Course 1		8:40 - 10:20 LVT Low Voltage Power Devices	8:40 - 10:20 SiC-4 Gallium Oxide and Diamond Devices	8:40 - 10:20 HV-2 Multi-Gate Technology and SJ Devices
9:30	9:30 - 10:20 Short Course 2	9:00 - 10:20 Plenary Session			
10:00	10:20 - 10:50 Coffee	10:20 - 10:50 Coffee	10:20 - 10:50 Coffee	10:20 - 10:50 Coffee	10:20 - 10:50 Coffee
10:30	10:50 - 11:40 Short Course 3	10:50 - 12:30 HV-1 New Power Device Designs and Gate Control Method	10:50 - 12:30 ICD Power IC Design	10:50 - 12:30 SiC-2 Design Approaches and Physics for Reliability and Performance of SiC Devices	10:50 - 12:30 SiC-3 Novel Devices and Ruggedness of SiC
11:00					
11:30	11:40 - 12:30 Short Course 4				
12:00					
12:30	12:30 - 14:00 Lunch	12:30 - 14:00 Lunch	12:30 - 14:00 Lunch	12:30 - 14:00 Lunch	12:30 - 14:00 Lunch
13:00					
13:30					
14:00	14:00 - 14:50 Short Course 5	14:00 - 15:40 SiC-1 Performance of Superjunction SiC devices	14:00 - 15:20 GaN-2 GaN Power Device Reliability and Tests	14:00 - 15:40 PK Packaging Technologies	14:00 - 15:20 GaN-3 Novel GaN Power Device and Technologies 2
14:30					
15:00	14:50 - 15:40 Short Course 6		15:20 - 15:40 Coffee		15:20 - 15:50 Closing Session
15:30	15:40 - 16:30 Short Course 7	15:40 - 16:10 Coffee		15:40 - 16:00 Coffee	
16:00		16:10 - 17:50 GaN-1 Novel GaN Power Device and Technologies 1	15:40 - 17:40 Poster Session 1 LVT/ICD/GaN	16:00 - 18:00 Poster Session 2 HV/PK/SiC	
16:30	16:30 - 17:00 Coffee				
17:00	17:00 - 19:00 Industrial Session				
17:30					
18:00					
18:30					
19:00		Welcome Reception	AdCom Meeting (Invitation Only)	Banquet Hall of Fame	TPC Meeting (Invitation Only)
19:30					
20:00					
20:30					
21:00					

Recording and Photography Policy

IEEE policy prohibits video recording or photographing of presentations unless permission from the presenter is obtained in advance. Photographing of people or social events is permitted.



WiFi

Free Wi-Fi is available for participants to use.
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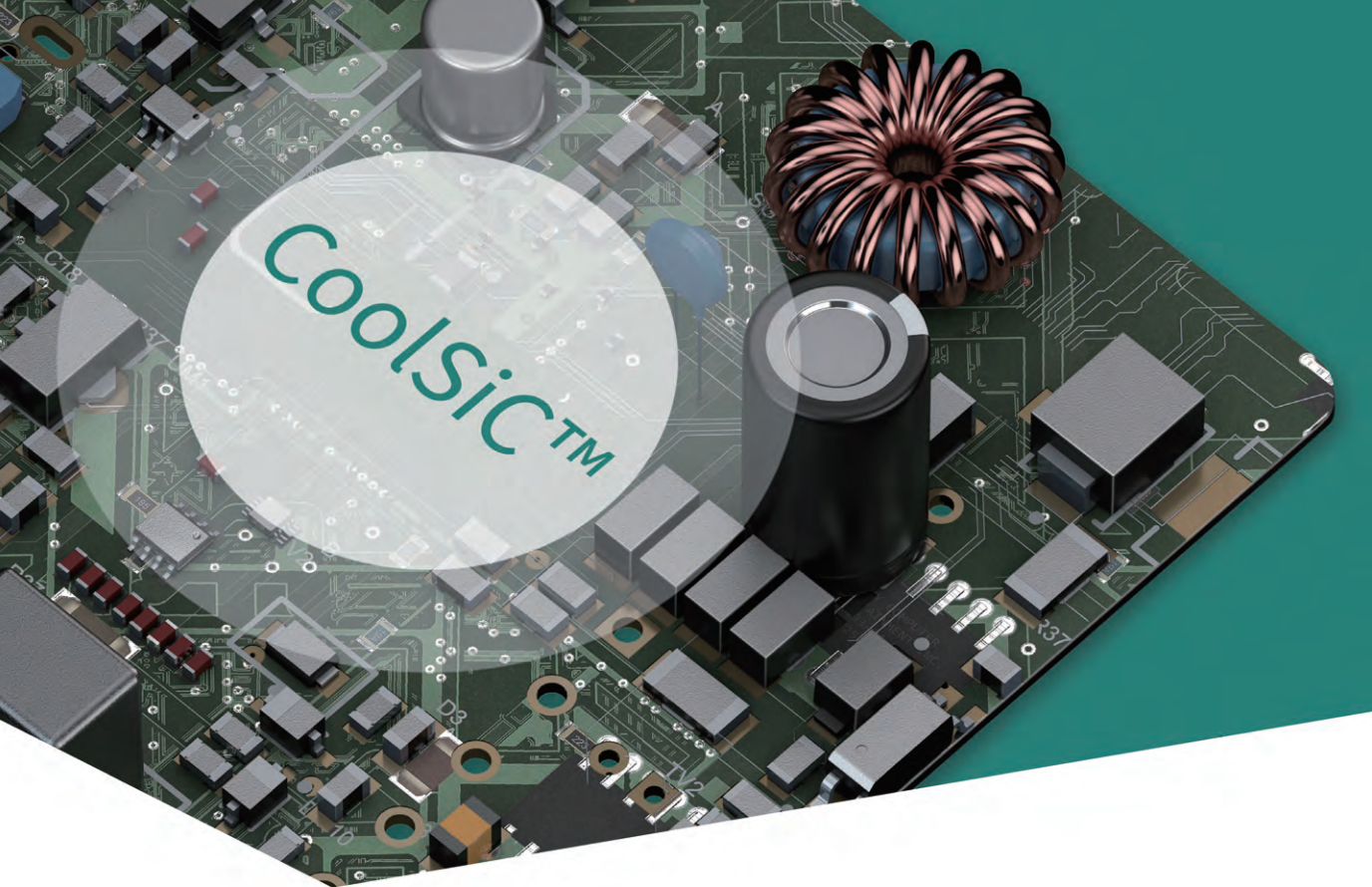
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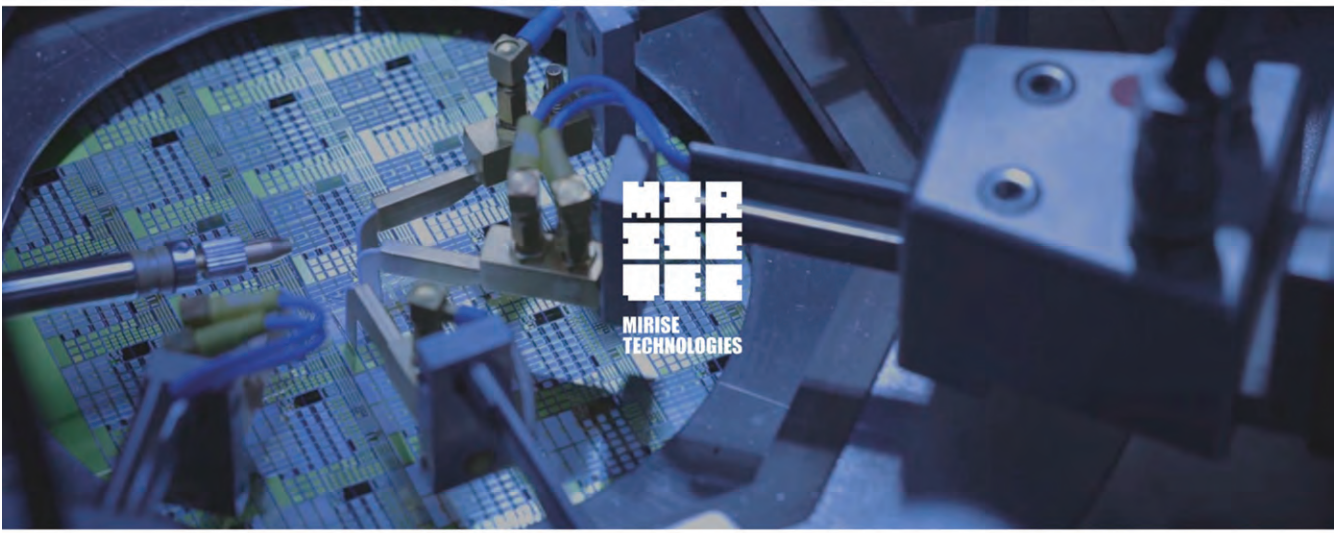


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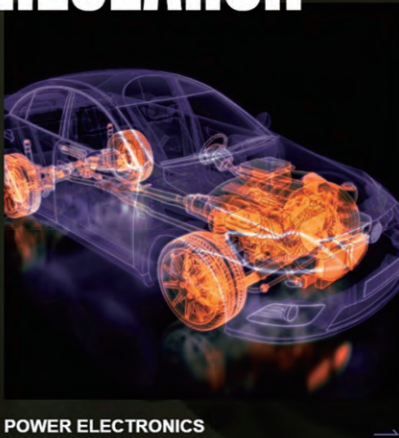




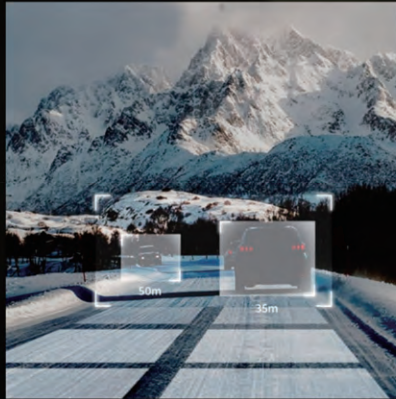
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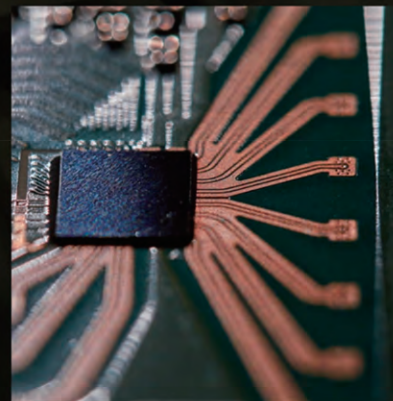
RESEARCH



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MESSAGE FROM THE CHAIR

As the General Chair of ISPSD, I sincerely hope that all participants will enjoy this conference as a special and inspiring time. ISPSD is not only a technical conference, but also a place where people from different countries, regions, companies, and universities can come together to freely discuss and share their experiences. I believe that the true value of ISPSD lies in this open and friendly atmosphere, where mutual understanding can grow. I hope this conference will be a meaningful and memorable experience for every power semiconductor specialist.

This kind of ISPSD has been made possible thanks to the continuous efforts of many people who supported past conferences—especially the former General Chairs, Technical Program Chairs, organizing committee members, and sponsors. Before ISPSD was established around 1990, the field of power semiconductor device technology was not clearly defined. It was often considered part of the broader semiconductor field, including LSI, or as a component of power electronics. The pioneers who founded ISPSD made great efforts to create an international conference focused on power semiconductor device technology—and they succeeded in establishing a new and distinct technical field, as well as the ISPSD community. I would like to express my deep appreciation to all those who contributed to past ISPSDs.

New challenges are also important for ISPSD to maintain and grow the community. One such challenge this year is the introduction of the full paper submission scheme. This change was made to improve the quality of the review process and to shorten the time from submission to presentation. I understand that this required significant effort from the Technical Program Committee, and I would like to express my sincere thanks to all the committee members for their great efforts.

I would also like to mention the Short Course. This year, we invited lecturers from various countries and regions to give compact and informative talks on advanced technologies related to power semiconductors. I hope many of you will join and enjoy the course.

Another highlight of this year's ISPSD is the strong connection with industry. We have 30 company exhibition booths, along with an Industry Session where companies will introduce their latest technologies.

This year, ISPSD is fully sponsored by the Institute of Electrical Engineers of Japan (IEEJ), with technical co-sponsorship from IEEE EDS, PELS, and IAS. We also received strong support from Kakenhi and NICT grants, and many companies kindly supported us as sponsors. I am very thankful for their contributions.

Welcome to ISPSD 2025 in Kumamoto and enjoy the conference!

Ichiro Omura
General Chair, ISPSD 2025

ORGANIZATION

ORGANIZING COMMITTEE

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GENERAL INFORMATION

Conference Venue

Kumamoto-Jo (Castle) Hall
3-40, Sakuramachi, Chuo-ku, Kumamoto-city, Kumamoto, 860-0805
TEL: +81-96-312-3737 FAX: +81-96-312-3738

Registration

In order to participate in the ISPSD 2025 conference, you must register online for the conference at www.ispsd2025.com using your credit card.

Registration Fees – Symposium

	Early registration until April 9, 2025 23:59 JST	Regular registration from April 10, 2025
IEEE/IEEJ Member	100,000 JPY	110,000 JPY
Non-member	110,000 JPY	120,000 JPY
Student IEEE/IEEJ Member*	60,000 JPY	65,000 JPY
Student Non-member*	65,000 JPY	70,000 JPY

Additional tickets for banquet and welcome reception:

Welcome Reception: 5,000 JPY/ticket

Banquet: 20,000 JPY/ticket

Each participant can purchase up to two additional tickets for their accompanying persons.

Registration Fees – Short Course

	Early registration until April 9, 2025 23:59 JST	Regular registration from April 10, 2025
IEEE/IEEJ Member	40,000 JPY	45,000 JPY
Non-member	45,000 JPY	50,000 JPY
Student IEEE/IEEJ Member*	25,000 JPY	30,000 JPY
Student Non-member*	30,000 JPY	35,000 JPY

Applicants must be full-time students at the time of the Conference and need to upload their valid student ID card scanned from both sides or another proof of full-time study.

Note: Payments must be received by the corresponding deadlines (early or regular), otherwise the subsequent rate will be automatically applied.

The registration fee includes:

Participant

Session (June 2-5, 2025)
Exhibition (June 2-5, 2025)
Lunch/Coffee (June 2-5, 2025)
Welcome Reception (June 2, 2025)
Banquet (June 4, 2025)
Proceedings (Online)
Industrial Session (June 1, 2025)

Student

Session (June 2-5, 2025)
Exhibition (June 2-5, 2025)
Lunch/Coffee (June 2-5, 2025)
Welcome Reception (June 2, 2025)

Proceedings (Online)
Banquet is not included and can be purchased separately (20,000 JPY)
Industrial Session (June 1, 2025)
Short Course (June 1, 2025)

Short Course Attendance
Short Course Printed Handout
Coffee Breaks, Lunch
Industrial Session

Methods of Payment

Registration fees must be paid in JPY:
Credit Card Only

Receipt

Receipt will be available from the registrants' MyPage after 19 May, 2025

Cancellations and Refunds

The ISPSD 2025 Secretariat must be notified in writing by e-mail at ISPSD2025@c-linkage.co.jp in the conference of the cancellation of the registration. Cancellation by phone call will not be accepted. The appropriate refunds will be made after the conference.

The following cancellation conditions apply:

Cancellations received	Refund
until April 9, 2025:	full refund of the registration fee
April 10 - 30, 2025:	50 % of the registration fee
from 1 May 2025:	no refund

In case of any change in registration, Convention Linkage, Inc. reserves the right to charge a 5,000 JPY handling fee.

In case of cancellation of the conference due to force majeure, Convention Linkage, Inc. reserves the right to charge a 5,000 JPY handling fee.

Name Change

No name change is accepted.

Recording and Photography Policy

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PRESENTER INSTRUCTIONS

Instructions for Oral Speakers

Presentation time

Oral papers presentation time is 15 minutes for presentation plus 5 minutes for Q&A, total 20 minutes.
All speakers are strictly requested to keep the time of their presentation.

Venue

Main Hall on the 4th floor.
Presenters should be at the standby seat that will be located in the front row of the seats before their session start time.

How to prepare presentation slides

The presentation slides should be prepared in 16:9 format by Microsoft PowerPoint (2013 or higher) or PDF. Only fonts included in the basic installation of MS-Windows (English version) are available. Recommended fonts are: Century, Century Gothic, Arial, Times New Roman, Tahoma, and Calibri. Do NOT use special characters.
Embedding pictures (GIF, PNG and BMP) or videos (WMV and MP4) into the slides is accepted, but do not increase the file size by unnecessarily high resolution material.

How to submit presentation slides at the conference

The presentation slides should be uploaded to an on-site PC from your USB stick and check properly working before start of the previous session at the latest.
(e.g. for a session starting at 10:50, it should be done by 8:40 at the latest)
Your own computer is NOT allowed for the presentation.
If you have any inconvenience with data transfer via USB stick, please contact the secretariat.

Instructions for Poster Presenters

Presentation time

LVT/ICD/GaN category: 15:40 - 17:40 on Tuesday, June 3
HV/PK/SiC category: 16:00 - 18:00 on Wednesday, June 4
Poster presenters are requested to present in front of their poster and answer questions during the entire session time.

Venue

A3 and A4 Conference Room on the 3rd floor.

How to prepare a poster

The poster must be prepared in PORTRAIT style. The recommended dimensions are 84.1 × 118.9 cm wide (format A0).
Do NOT exceed the overall dimensions of the poster board (210 cm high by 90 cm wide).

Set-up and Dismantling time

All posters are required to be displayed during the entire conference period from June 2 to 5.
Set-up: by 14:00 on Monday, June 2
Dismantling: from 12:00 until 15:00 on Thursday, June 5

The location of posters will be indicated by ID number of the paper on boards

Fixing material (Tape etc.) will be available in the poster presentation venue.
Posters not removed after the dismantling period will be discarded by the secretariat and will not be sent back to the author.

SOCIAL EVENTS

Monday Welcome Reception

Date & Time: Monday, June 2, 18:00–20:30

Venue: Civic Hall, 2nd Floor of Kumamoto-Jo (Castle) Hall

Admission:

Symposium participants: Included in registration fee

Accompany person: Additional ticket required

Dress Code: No specific dress code

Banquet

Date & Time: Wednesday, June 4, Door Open 18:30, Start 19:00

Venue: Banquet Hall "Aso", 5th Floor, Hotel Nikko Kumamoto

Admission:

Symposium participants: Included in registration fee

(Not included in student registration)

Accompany person: Additional ticket required

Dress Code: No specific dress code



LUNCH

During the conference: Lunch time

Venue: Civic Hall, 2nd Floor of Kumamoto-Jo (Castle) Hall

Admission: Symposium participants

ISPSD 2024 OHMI BEST PAPER AWARD

Development of Vertical-Channel Fin-SiC MOSFET for 3.3 kV applications

Tomoka Suematsu^{1,2}, Takeru Suto¹, Yuki Mori¹, Haruka Shimizu¹,
Yasunori Tanaka² and Akio Shima¹

¹*Research and Development Group, Hitachi, Ltd., Kokubunji, Tokyo, Japan*

²*National Institute of Advanced Industrial Science and Technology, Tsukuba, Ibaraki, Japan*

Abstract:

We have developed a 3.3 kV SiC Vertical-Channel Fin MOSFET, original structure named VC Fin-SiC. VC Fin-SiC features a fin-shaped channel and a JFET region arranged perpendicularly beneath the fin, allowing for increased designability and scalability. This structure increases the number of JFETs and channels per active area while protecting trench corners with a P-region. The JFET structure was optimized using TCAD simulation to achieve low on-resistance and high reliability. Evaluation of static and switching properties demonstrated that VC Fin-SiC can achieve a 30% reduction in on-resistance while maintaining a high threshold voltage, and a 30% reduction in switching loss due to fast turn-on compared to DMOS. Through this research, we discovered the significance of designing the channel and JFET regions, even at high voltages where drift layer resistance is typically dominant.



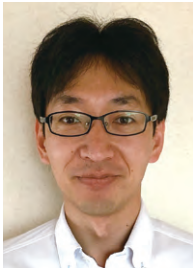
Tomoka Suematsu received the B.S. degree from Hiroshima University in 2017 and the M.S. degree from Kyoto University in 2019. Since 2019, she has been working as a researcher at Hitachi, Ltd., and since 2021, also working at the National Institute of Advanced Industrial Science and Technology (AIST). Her research focuses on developing SiC power semiconductor devices and power electronics.



Takeru Suto received the B.E. degree in 2015 and the M.E. degree in 2017 from Tokyo Institute of Technology (now known as the Institute of Science Tokyo). He has been working as a researcher with the R&D group at Hitachi, Ltd. since 2017. His research interests include silicon carbide power semiconductor devices, device modeling, machine learning techniques, and diamond crystal growth for quantum devices.



Yuki Mori received the B.S. and M.S. degrees in physics from Keio University in 1996 and 1998, respectively, and the Ph.D. degree from the University of Tokyo in 2014. In 1998, she joined the Central Research Laboratory, Hitachi, Ltd. From 1998 to 2009, she worked on VLSI device and process technology, especially in charge of the reliability analysis in dynamic random-access memories. Since 2010, she has been working on developing silicon carbide power devices. Her current research interests include the reliability of power devices.



Haruka Shimizu received the B. E. and M. E. degrees in material science from the University of Tokyo in 2003 and 2005 respectively, and received the Ph. D degree from Tsukuba University in 2020. In 2005, he joined the Central Research Laboratory at Hitachi, Ltd. His work has focused on advancing technologies related to SiC SBD, JFET, and MOSFET, contributing to the field of power semiconductor innovation.



Yasunori Tanaka received the Ph.D. degree in electronic engineering from Osaka University in 1996. In 1996, he joined the Quantum Radiation Division at Electrotechnical Laboratory. Since 2001, he has been working in the National Institute of Advanced Industrial Science and Technology conducting research on SiC power devices.



Akio Shima received the B. E. and M. E. degrees in applied physics from the University of Tokyo in 1993 and 1995 respectively, and received the Ph. D degree from Waseda University in 2008. He is now working as a Distinguished Researcher in Research & Development Group, Hitachi, Ltd., responsible for research activities on Energy Conversion Electronics including SiC power electronics and its industrial application.

ISPSD 2024 CHARITAT YOUNG RESEARCHER AWARD

An Enhancement-mode AlGaIn/GaN HEMT with Island-Ohmic p-GaN featuring stable threshold voltage and large gate swing

Xinyue Dai^{1,2}, Qimeng Jiang^{1,2}, Chao Feng³, Zhongchen Ji^{1,2}, Sen Huang^{1,2}, Runxian Xing⁴, Guohao Yu⁴, Xinguo Gao¹, Xinhua Wang^{1,2}, Xinyu Liu^{1,2}

¹*Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, China*

²*University of Chinese Academy of Sciences, Beijing, China*

³*Shenzhen Pinghu Laboratory, Shenzhen, China*

⁴*Suzhou Institute of Nano-Tech and Nano-Bionics, Suzhou, China*

Abstract:

A novel AlGaIn/GaN HEMT based on an Island-Ohmic p -GaN gate (IO-PGaN) structure is proposed. Thanks to the Island-Ohmic, the “floating” p -GaN is connected with the gate terminal via the heavily doped p^{++} -GaN island. Therefore, the net charges generated in the p -GaN region under the gate or drain stress conditions, could be easily compensated by supplying holes via the ohmic gate structure, resulting in a stable threshold voltage (V_{TH}). Meanwhile, a SiO_2 side wall is intentionally formed to achieve a moderate E -field at the island corner, and a JFET-like structure formed by the Schottky-metal/ p -GaN junction delivers a self-limited gate leakage.



Xinyue Dai obtained the Ph.D. degree from the University of Chinese Academy of Sciences (Institute of Microelectronics, CAS) in 2024, where her research focused on the fabrication and optimization design of p -GaN power devices. Currently, she is working at Shenzhen Pinghu Laboratory as an Assistant Researcher. Her current research interests include the modeling and optimization of GaN HEMTs and related device technologies..

ISPSD 2024 BEST POSTER AWARD

1-kV β -Ga₂O₃ UMOSFET with Quasi-Inversion Nitrogen-Ion-Implanted Channel

Qi Liu¹, Xuanze Zhou¹, Man Hoi Wong², Huidong Yao¹, Jingbo Zhou¹, Xiaodong Zhang³,
Guangwei Xu¹, Shibing Long¹

¹*School of Microelectronics, University of Science and Technology of China, Hefei, China*

²*Department of Electronic and Computer Engineering, Hong Kong University of Science and
Technology, Hong Kong, China*

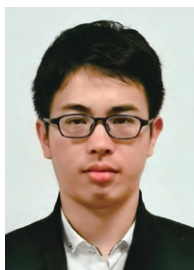
³*Suzhou Institute of Nano-Tech and Nano-Bionics, Chinese Academy of Sciences, Suzhou, China*

Abstract:

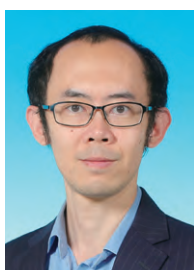
We demonstrated 1-kV vertical enhancement-mode β -Ga₂O₃ U-shaped trench gate metal-oxide-semiconductor field-effect transistors (UMOSFETs) with nitrogen-ion-implanted channel. The nitrogen-ion-implanted region serves as a current blocking layer (CBL) and also allows a quasi-inversion channel to form at the trench sidewall. The activation annealing temperature of the nitrogen-ion-implanted CBL was optimized to suppress the leakage current. The CBL annealed at higher temperature exhibits better current blocking capability than its counterpart annealed at lower temperature. Based on the CBL annealed at higher temperature, the UMOSFET exhibits an improved on-off ratio of $\sim 10^6$, an on-resistance of $87.6 \text{ m}\Omega \cdot \text{cm}^2$ and a remarkable breakdown voltage of 1028 V. This is the first 1-kV β -Ga₂O₃ MOSFET based on CBL, showing the potential of β -Ga₂O₃ UMOSFETs with nitrogen-ion-implanted channel for kilovolt-class applications.



Qi Liu received the B.E. degree from Jiangnan University, Wuxi, China in 2020. She is currently pursuing the Ph.D. degree with the School of Microelectronics, the University of Science and Technology of China (USTC), Hefei, China. Her research mainly focuses on the design, optimization and characterization of gallium oxide power transistors.



Xuanze Zhou received his PhD from the University of Science and Technology of China (USTC) in 2023 and continued as a postdoctoral researcher at the same institution. Since 2018, his research has centered on gallium oxide-based power MOSFETs. Following his graduation, his interests expanded to include gallium oxide materials, defect characterization, MOCVD growth, and power MOSFET development.



Man Hoi Wong received the B.S. degree from Cornell University in 2004 and his Ph.D. degree from the University of California Santa Barbara in 2009. From 2013 to 2019, he developed Ga₂O₃ power devices at Japan's National Institute of Information and Communications Technology. Currently, he is an associate professor of Electronic and Computer Engineering at the Hong Kong University of Science and Technology, where he engages in fundamental and applied research of ultrawide-bandgap semiconductors such as Ga₂O₃.



Huidong Yao received the B.S. degree from Nanjing University of Science and Technology, Nanjing, China in 2022. She is currently pursuing the Ph.D. degree with the School of Microelectronics, the University of Science and Technology of China, Hefei, China. Her research mainly focuses on the design, fabrication, and characterization of current blocking layers in gallium oxide for high-power electron devices.



Jingbo Zhou received the B. S. degree from University of Science and Technology of China, China, in 2023. Currently, he is a doctoral student studying characterizations of compensation doping for power devices on gallium oxide at University of Science and Technology of China and a visiting student at Sorbonne University. He is also working on establishing an analytical model of gallium oxide power transistors through electrical and magnetic properties.



Xiaodong Zhang received the Ph.D. degree from the University of Science and Technology of China, Hefei, China, in 2022. He is currently a Professor with the Suzhou Institute of Nano-Tech and Nano-Bionics (SINANO), Chinese Academy of Sciences (CAS), Suzhou, China. His main research interests include the epitaxial growth of ultrawide bandgap semiconductor gallium oxide and Aluminum Nitride films, power and optoelectronic devices, etc.



Guangwei Xu received his PhD from the Institute of Microelectronics of the Chinese Academy of Sciences in 2017. Then, he joined the University of California, Los Angeles as a postdoc. He joined the University of Science and Technology of China as a research fellow in the Shibing Long Group in 2019. His research focuses on wide bandgap semiconductor power device fabrication, device defect state measurement and device modeling.



Shibing Long is a full professor at the School of Microelectronics, University of Science and Technology of China. He received his PhD from the Institute of Microelectronics of the Chinese Academy of Sciences in 2005. Then, he worked there from 2005 to 2018 and joined the University of Science and Technology of China in 2018. His research focuses on micro- and nanofabrication, RRAM, ultrawide bandgap semiconductor devices (power devices and detectors) and memory circuit design.

ISPSD HALL OF FAME

Michael S. Adler for his contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences

Gehan Anil Joseph Amaratunga for his contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences

B. Jayant Baliga for his contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences

Xingbi Chen* for his contributions to superjunction power semiconductor devices

Tat-Sing Paul Chow for his contributions to silicon and wide bandgap power semiconductor devices, and his leadership role in organizing ISPSD conferences

Claudio Contiero for his contributions to the proliferation of BCD technologies, and to the ISPSD conferences

Mohamed Darwish for his contributions to the advancement of power semiconductor technology, and his leadership role in organizing ISPSD conferences

Don Disney for contributions to power IC technology, and his leadership role in organizing ISPSD conferences

Taylor R. Efland for his contributions to power IC technology, and his leadership role in organizing ISPSD conferences

Wolfgang Fichtner for his contributions to MOS gated thyristors and TCAD modeling tools, and his leadership role in organizing ISPSD conferences

Tatsuhiko Fujihira for his contributions to superjunction power semiconductor technologies and industrialization of power semiconductor devices

Min-Koo Han for his contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences

Oliver Häberlen for his contributions to trench MOSFET and power GaN technology, and for his outstanding leadership in organizing ISPSD 2020 during the pandemic

Phil Hower for his contributions to power device safe operating area study and power IC technology

André A. Jaecklin for his contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences

Daniel Kinzer for his contributions to power MOSFET technology, and his leadership role in organizing ISPSD conferences

Thomas Laska for his contributions to IGBT technology and devices

Alex Lidow for contributions to silicon and GaN power device technology

Leo Lorenz for his contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences

Gourab Majumdar for his contributions to IGBT and intelligent power module technology, and his leadership role in organizing ISPSD conferences

Hiroyuki Matsunami for his contributions to the developments of silicon carbide epitaxial technology and wide bandgap power semiconductor devices

José Millán* for his contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences

Peter Moens for his contributions to integrated power technology and GaN power device and reliability, and his leadership role in organizing ISPSD conferences

Mutsuhiro Mori for his contributions to high voltage insulated gate bipolar transistor for traction and high voltage systems, and his leadership role in organizing ISPSD conferences

Akio Nakagawa for his contributions to IGBT and power IC technology

Hiromichi Ohashi for his contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences

Tadahiro Ohmi* for his contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences

Masahiro Okamura for his contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences

John Palmour* for his contributions to SiC technology and devices

James Plummer for his contributions to MOS-bipolar power devices and power ICs, and for inspiring and training a new generation of device researchers

C. Andre T. Salama for his contributions to power IC technology, and his leadership role in organizing ISPSD conferences

Yasukazu Seki for his contributions to IGBT technology, and his leadership role in organizing ISPSD conferences

John Shen for contributions to high-frequency power MOSFET and leadership role in organizing ISPSD

Kuang Sheng for his contributions to SiC power device technology, and his leadership role in organizing ISPSD conferences

M. Ayman Shibib for his contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences

Dieter Silber for his contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences

Johnny Sin for his contributions to the design and commercialization of power semiconductor devices and his leadership role in organizing ISPSD conferences

Jan Šonský for his contributions to GaN device technology, and his leadership role in organizing ISPSD conferences

Paolo Spirito for his contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences

Yoshitaka Sugawara for his contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences

Yoshiyuki Uchida for his contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences

Florin Udrea for inspiring a generation of engineers to excel in power semiconductors and his numerous contributions to the field and to ISPSD

Daisuke Ueda for his work on trench structure MOS devices and GaN devices

Harry Vaes for his contributions to RESURF technology

Jan Vobecký for pushing the limits of diodes and thyristors by carrier lifetime engineering

Carl Frank Wheatley* for his contributions to IGBT and radiation-hard power device technology

Richard K. Williams for his contributions to trench power MOSFET and power IC technology, and his leadership role in organizing ISPSD conferences

Toshiaki Yachi for his contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences

*Deceased member

PLENARY TALKS

Main Hall (4th Floor)
Date: June 2 (Monday) 9:00-10:20

Gallium Nitride; Past, Present and Future in an Ever-Changing Market

Prof. Umesh Mishra, *ECE Department, UC Santa Barbara, CA, USA*

Gallium Nitride is a very exciting solution for many power electronics applications as the market continues to evolve and, in many ways, may emerge as even more important than Si and SiC. The primary reason remains its superior materials properties, most importantly the high mobility that is afforded by the AlGaN/GaN heterojunction. Lateral GaN power devices are attractive because the full region that holds voltage is a high electron mobility region and it is uniquely capable of delivering bidirectional voltage blocking, important in many applications including, solar inverters, chargers and motor drives. Lateral devices are also amenable to integrating smart functionality with the device. The drawback of a lateral device is a larger chip size and the need for field plates to manage fields, issues that can be mitigated with superjunction technology, now being investigated by multiple research institutions. Vertical GaN devices, on the other hand, are attractive for small chip-size and high-voltage rating, but have significantly lower electron mobility and require low dislocation density bulk substrates for reliable operation, which can increase cost. In this talk we will go over the history of GaN device evolution for power electronics applications and make predictions for the future.

Chuo Shinkansen with Superconducting Maglev and Semiconductor Power Conversion

Mr. Junichi Kitano, *Central Japan Railway Company, Japan*

The Chuo Shinkansen is a high-speed mass transport system that will connect Tokyo, Nagoya and Osaka in about one hour at a speed of 500 km per hour. Construction is currently underway between Shinagawa and Nagoya as a successor to the Tokaido Shinkansen.

The superconducting maglev levitates 10cm without control due to the dynamic electromagnetic induction between the superconducting magnets mounted on the vehicle and the levitation and guidance coils on the ground, and travels at ultra-high speeds of 500km/h inside a U-shaped concrete guideway. The key to the levitation and travel of the superconducting maglev is the strong magnetic force of the superconducting magnets and linear motor technology. The superconducting magnets are used in common with the field magnets of the linear synchronous motors, and each side of the vehicle constitutes a different motor.

The 16-car train has a capacity of approximately 1,000 passengers and is a large-capacity transportation system that can run more than eight trains per hour. Compared to general railways that use steel wheels and run on rails, there is no restriction of friction (adhesion) between wheel and rail, which allows for ultra-high speeds and high acceleration and deceleration, so there is a high utilization rate of the vehicles and the advantage that mass transportation can be achieved with a small number of trains.

Ten mainline substations will be installed between Shinagawa and Nagoya. Each substation will have six 60MVA inverters on double tracks, and installation of converters is already underway at some substations.

Thus, semiconductor power conversion is a key technology for superconducting maglev, and since the emergence of large-capacity thyristors, it has grown together with new semiconductor power devices such as light-triggered thyristors, GTOs, IGBTs, GCTs, and IEGTs.

Also, Dynamic WPT is used to supply around 1MW of auxiliary power to vehicles that levitate without contact, and here too high-frequency semiconductor power conversion technology is important. The advent of SiC semiconductors has made it possible to build efficient systems.

Innovative superconducting maglev technology is not unique to Japan. We hope that this new transportation system, which will connect Tokyo and Osaka in just one hour, will bring new possibilities to the world.

SHORT COURSE

Venue: Civic Hall (2nd Floor) Date: June 1 (Sunday) 8:30-16:30

Short Course Chair: Dr. Tatsuya Nishiwaki, *Toshiba Electronic Devices & Storage, Japan*

SC1: 200mm SiC Substrate development and 300mm SiC opportunities & challenges

Dr. Chao Gao, *SICC, China*

Abstract: Technical development of large-sized SiC substrates will be presented in the meeting. Progress of 200 mm SiC substrate in volume production as well as the technical focus from both material and device side will be elaborated.

Besides, 300 mm SiC substrates is developed and the progress will be presented. The challenges and opportunities of 300 mm in the industry is to be discussed.

SC2: Technology for p-GaN gate High-voltage Gallium Nitride Transistors

Mr. Yasuhiro Uemoto, *Infineon Technologies, Japan*

Abstract: GaN power devices are basically normally on devices that take advantage of the superior material properties of 2DEG and high mobility due to the AlGaIn/GaN heterostructure. This is a great gift from the nature. However, in actual use, normally off devices are strongly desired, and as a result of the challenges by many researchers, normally off structures with p-GaN gate become the mainstream in the market. In recent years, GaN has encountered chargers in the consumer market as a killer application, and the market has begun to expand. However, in the near future, in addition to the consumer market, there is no doubt that markets requiring more reliable devices, such as industrial and automotive, will expand drastically. This session will go back to the basics to explain the benefits and technologies of GaN power devices. E-mode GaN and d-mode GaN technologies will be outlined as well as a comparison of p-GaN gates in GIT and Schottky structures. In addition, Dyn Rdson behavior related to C in GaN buffers will be presented.

SC3: Overview of Silicon Power Devices: History, Trends and Outlook

Prof. Wataru Saito, *Kyushu University, Japan*

Abstract: The power device market has been steadily expanding toward carbon neutrality, and continuous growth is expected in the future. While wide-bandgap semiconductor power devices, such as SiC and GaN, have been commercialized and are experiencing rapid market growth, they have yet to surpass silicon power devices in market share. Even in 2030, silicon power devices are projected to account for more than 80% of the market.

In this lecture, an overview of silicon power devices, covering their history, trends, and future outlook, is provided. One key aspect of power electronics development is the increasing power density of systems. Power device performance improvements have significantly contributed to this trend, and the evolution of device structures and advancements in process technologies that have driven these improvements are discussed. Additionally, recent R&D efforts aimed at further enhancing performance, as well as the transition to larger wafer diameters of 300 mm to expand production capacity, are introduced.

SC4: Recent Requirements and Trends on Power IC Technology

Dr. Sang Gi Lee, *DB HiTek, South Korea*

Abstract: The power IC market is projected to grow from 2025 to 2028 at a CAGR of 4.1% (Omdia, 2025). As the market expands and product diversity increases, the requirement for the device and process option supported by BCD (Bipolar-CMOS-DMOS) technology is becoming more critical, not only for maintaining cost-competitiveness but also for enhancing functionality. Therefore, competition is intensifying around differentiated device

performance, value-added process options, and design-friendly PDK features.

This presentation will discuss power device performance, figures of merit, challenges in process integration, and the new PDK capabilities required by recent BCD technology. First, we will explore the performance requirements of LDMOS, a core component of Power ICs, across different applications, strategies for achieving target performance, key reliability aspects, and evaluations of large-size LDMOS devices comparable to discrete components. Next, we will discuss isolation schemes and special process options, such as HV capacitor, galvanic isolation, and embedded ReRAM. Finally, we will briefly cover the latest PDK features in modeling, ESD solutions, and P-cell.

SC5: Power Electronics Design Automation Tools: Steps towards Realization

Dr. Tristan Evans, *PE-Systems, Germany*

Abstract: The methods employed in designing power systems must be reconsidered as new semiconductor devices and technologies continue to proliferate. Modern design engineers are faced with an accelerating growth in power electronics applications, yet their ranks do not scale at the same rate. Compounding this, the traditional design flow for components and converters follows highly iterative, manual, intensive, and time-consuming cycles. The neighboring field of VLSI solved many of these problems by developing electronic design automation (EDA) tools in the 80s. This short course will explore ways in which EDA tools for power electronics are beginning to introduce new design flows—exploring more possibilities in shorter time. Also addressed will be ways to improve quality and quantity of component data and better ways to distribute it among trusted partners so that machine learning and AI-driven design techniques can be fully realized.

SC6: AI-assisted Reliability Testing, Modeling, and Condition Monitoring for Power Semiconductor Modules

Prof. Huai Wang, *Aalborg University, Denmark*

Abstract: With an increasing percentage of electricity being processed by power electronic converters, optimizing efficiency and reliability is critical for affordable, secure, and sustainable energy systems. Power semiconductor modules have been widely used for power electronic converters. Therefore, its reliability performance, both qualitative and quantitative aspects, is of critical importance. Artificial Intelligence (AI) is increasingly solving optimization, regression, and classification problems within the energy sector, where deep electrification and digitalization intersect. This short course focuses on the application of AI in the reliability aspect study of semiconductor modules for power electronics, including AI-assisted reliability testing for testing time reduction, fast dynamic thermal modeling, and condition monitoring for predictive maintenance. A few case studies will be introduced to demonstrate how AI can assist in addressing the challenges in power semiconductor module reliability research.

SC7: Chip Embedded Power Package Technologies for AI and Vehicles

Mr. Yoshiaki Aizawa, *AOI ELECTRONICS, Japan*

Abstract: In the field of semiconductor power packaging, wiring resistance and inductance have become a major concern for increasing power and switching frequency. Especially in AI/Data Center and EV applications, package inductance has a critical impact on power integrity, switching noise generation and switching uniformity. This power integrity also affects signal integrity and ultimately degrades processor chip performance in AI/Data Center application. Chip-embedded packages have attracted much attention in recent years as a promising solution to these issues. This course will introduce the development history, technical features, and development roadmap of the chip-embedded power package, in particular the panel-level package for AI/Data Center and EV.

TECHNICAL PROGRAM

MONDAY, JUNE 2, 2025

8:30 - 9:00

4F Main Hall

Opening Session

Opening Remarks

Ichiro Omura, General Chair

Kyushu Institute of Technology, Japan

ISPSD 2024 Ohmi Best Paper Award

Nando Kaminski, General Chair of ISPSD 2024

University of Bremen, Germany

Ulrike Grossner, Technical Program Committee Chair of ISPSD 2024

ETH Zurich, Switzerland

Program Introduction

Yuichi Onozawa, Technical Program Committee Chair

Fuji Electric, Japan

9:00 - 10:20

4F Main Hall

Plenary Session

Chairs: Ichiro Omura (*Kyushu Institute of Technology, Japan*)

David Sheridan (*Alpha & Omega Semiconductor, USA*)

9:00 - 9:40

Gallium Nitride: Past, Present and Future in an Ever-Changing Market

Umesh Mishra

ECE Department, UC Santa Barbara, CA, USA

9:40 - 10:20

Chuo Shinkansen with Superconducting Maglev and Semiconductor Power Conversion

Junichi Kitano

Central Japan Railway Company, Tokyo, Japan

10:20 - 10:50

3F A1/A2 Room and Foyer (Exhibition Area)

Coffee Break

10:50 - 12:30

4F Main Hall

HV-1: New Power Device Designs and Gate Control Method

Chairs: Wentao Yang (*HUAWEI Technologies, China*)

Karthik Padmanabhan (*Alpha & Omega Semiconductor, USA*)

10:50 - 11:10

Shallow Active Trench CSTBT™ with Low Switching Loss for 6.5kV Class

Kakeru Otsuka, Ayanori Gatto, Koji Tanaka, Shinya Soneda

Power Device Works, Mitsubishi Electric, Fukuoka, Japan

- 11:10 - 11:30 **Influence of IGBT Switching Behavior on Conducted and Radiated Emissions below 30 MHz**
 Yosuke Sakurai¹, Yasutoshi Yoshioka², Marco A. Azpúrua³, Jordi Solé-Lloveras³, Rik W. De Doncker⁴
¹Semiconductors Business Group, Fuji Electric, Matsumoto, Japan; ²Corporate R&D Headquarters, Fuji Electric, Tokyo, Japan; ³EMC Electromagnetic BCN, S.L., Barcelona, Spain; ⁴Institute for Power Electronics and Electrical Drives, RWTH Aachen University Aachen, Germany
- 11:30 - 11:50 **First demonstration of 6.5kV fully scaled IGBT with ultra-shallow edge termination (USET)**
 Takuya Saraya¹, Kiyoshi Takeuchi¹, Kazuo Itou¹, Toshihiko Takakura¹, Munetoshi Fukui¹, Shinichi Suzuki¹, Hiroyuki Takase¹, Wataru Saito², Shin-Ichi Nishizawa², Toshiro Hiramoto¹
¹The University of Tokyo, Tokyo, Japan; ²Kyushu University, Fukuoka, Japan
- 11:50 - 12:10 **A Novel 4.5 kV nonlatching IGCT for turn-on di/dt controllability without a clamp circuit**
 Gurunath Vishwamitra Yoganath¹, Jan Fuhrmann¹, Tobias Wikström², Hans-Günter Eckel¹
¹Institute for Electrical Power Engineering, University of Rostock, Germany; ²Hitachi Energy, Semiconductors, Switzerland
- 12:10 - 12:30 **New Bidirectional Asymmetric High Voltage TVS (Transient Voltage Suppressor) device**
 Boris Rosensaft¹, Xingchong Gu², Martin Schulz³
¹SBU Bipolar Chip R&D, IXYS Global Services GmbH, Lampertheim, Germany; ²PI&NPD Littelfuse Semiconductor, Wuxi, China; ³Semiconductor Power Applications, Littelfuse Europe GmbH, Bremen, Germany

12:30 - 14:00 **2F Civic Hall**
Lunch Break

14:00 - 15:40 **4F Main Hall**
SiC-1: Performance of Superjunction SiC devices
Chairs: Ulrike Grossner (ETH Zurich, Switzerland)
 Noriyuki Iwamuro (University of Tsukuba, Japan)

- 14:00 - 14:20 **Avalanche and Short Circuit Withstand Capabilities in 3.3 kV-class SiC Superjunction MOSFET**
 Shinichiro Matsunaga¹, Takeshi Tawara², Syunki Narita², Masakazu Baba², Kensuke Takenaka¹, Tadao Morimoto¹, Shinsuke Harada¹
¹Advanced Power Electronics Research Center, AIST, Tsukuba, Japan; ²Fuji Electric, Matsumoto, Japan
- 14:20 - 14:40 **Bipolar characteristics of 3.3kV-class 4H-SiC Epi-refilled Super-Junction Diodes**
 Haoyuan Cheng¹, Hengyu Wang¹, Chi Zhang¹, Jiangbin Wan¹, QianQian Que¹, Han Wang¹, Haoyu Wang¹, Ce Wang¹, Jingrui Han², Hungkit Ting², Kuang Sheng¹
¹College of Electric Engineering, Zhejiang University, Hangzhou, China; ²Tianyu Semiconductor, Guangdong, China

- 14:40 - 15:00 **Comparative Study on Charge-Imbalance Super Junction Termination for 3kV 4H-SiC Full-SJ and Semi-SJ Devices**
 Chi Zhang¹, Hengyu Wang¹, Haoyuan Cheng¹, Jiangbin Wan¹, Han Wang¹,
 Haoyu Wang¹, Ce Wang¹, Zijian Hu¹, Jingrui Han², Hungkit Ting², Kuang Sheng¹
¹College of Electrical Engineering, Zhejiang University, Hangzhou, China; ²Tianyu Semiconductor, Guangdong, China
- 15:00 - 15:20 **Investigation of static and dynamic behavior of silicon carbide semi-super-junction structure in Schottky barrier diodes**
 Hiroshi Kono, Katsuhisa Tanaka, Tsutomu Kiyosawa, Kenya Sano
 Toshiba Electronic Devices & Storage, Hyogo, Japan
- 15:20 - 15:40 **Comparative Study of Different Layouts for 1.7kV Charge-Balance-Assisted SiC MOSFETs**
 Yuhan Duan^{1,2}, Botao Sun³, Yuanlan Zhang³, Pan Liu^{1,2}, Guangyin Lei¹, Min Li¹,
 Qingchun Jon Zhang¹
¹Academy for Engineering and Technology, Fudan University, Shanghai, China; ²Research Institute of Fudan University in Ningbo, Ningbo, China; ³SiChain Semiconductors (Ningbo), Ningbo, China

15:40 - 16:10 **3F A1/A2 Room and Foyer (Exhibition Area)**
Coffee Break

16:10 - 17:50 **4F Main Hall**
GaN-1: Novel GaN Power Device and Technologies 1
Chairs: Tom Chun-Lin Tsai (TSMC, Taiwan)
 Akira Nakajima (AIST, Japan)

- 16:10 - 16:30 **First Demonstration of Optically-Controlled 650 V Power GaN HEMT with Ultrafast Switching Speed**
 Xin Yang¹, Liyang Jin², Matthew Porter³, Hongchang Cui¹, Zineng Yang¹, Hehe Gong¹,
 Han Wang¹, Linbo Shao², Yuhao Zhang¹
¹Department of Electrical and Electronic Engineering, The University of Hong Kong, Hong Kong, China; ²Bradley Department of Electrical and Computer Engineering, Virginia Tech, Blacksburg, USA; ³Center for Power Electronics Systems (CPES), Virginia Tech, Blacksburg, USA
- 16:30 - 16:50 **First Demonstration of a Fully-Vertical GaN Power finFET with Direct Optical Triggering**
 Jung-Han Hsia¹, Joshua Andrew Perozek¹, Joseph Park², Tomás Palacios¹
¹Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, MA, USA; ²MIT Lincoln Laboratory, Lexington, MA, USA
- 16:50 - 17:10 **Enhanced Photon-Generated Hole Spreading in p-GaN Gate Double-Channel HEMT for Suppression of Back-Gating Effect from Si Substrate**
 Zheng Wu, Tao Chen, Yat Hon Ng, Haochen Zhang, Zongjie Zhou, Yan Cheng,
 Hang Liao, Yutao Geng, Yumeng Huang, Kevin J. Chen
 Dept. of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong, China

- 17:10 - 17:30 **Low $R_{\text{ON}}Q_{\text{G}}$ 1.2 kV-Class Normally-Off GaN Gate Injection Transistor on GaN Substrate with Asymmetric Gate Structure**
Hiroyuki Handa, Naohiro Tsurumi, Masao Kawaguchi, Masahiro Ogawa,
Daisuke Shibata, Yoshio Okayama, Satoshi Tamura
Manufacturing Innovation Division, Panasonic Holdings, Osaka, Japan
- 17:30 - 17:50 **Beyond 650 V Dynamic Switching of High Voltage AlGaIn/GaN/AlN HEMTs on monocrystalline AlN Substrates**
Houssam Halhoul¹, Mihaela Wolf¹, Frank Brunner¹, Sven Besendörfer²,
Martin Damian Cuallo¹, Steffen Breuer¹, Gleb Lukin², Andreas Lesnik², Elke Meissner²,
Oliver Hilt¹
¹Ferdinand-Braun-Institut (FBH), Berlin, Germany; ²Fraunhofer Institute for Integrated Systems and Device Technology IISB, Erlangen, Germany

18:00 - 20:00 **2F Civic Hall**
Welcome Reception

8:40 - 10:20 4F Main Hall

LVT: Low Voltage Power Devices

Chairs: Atsushi Sakai (*Renesas Electronics, Japan*)

Raffaella Roggero (*STMicroelectronics, Italy*)

8:40 - 9:00

Current Sharing in Trench MOSFETs During Fast Switching Transients

Riccardo Tambone^{1,2}, Alessandro Ferrara¹, Filippo Magrini³, Raymond J.E. Hueting²

¹*Infineon Technologies Austria AG, Villach, Austria;* ²*University of Twente, Enschede, The Netherlands;* ³*Infineon Technologies AG, Neubiberg, Germany*

9:00 - 9:20

Polysilicon trench diode based on P-N junction

Lia Masoero¹, Rosalia Germana¹, Adriano Novarese¹, Alfio Scuderi², Monica Petralia², Alessandro Nodari¹, Patrick Calenzo¹

¹*Digital & Smart Power Techn. & Digital FE Manuf., VIPower R&D, STMicroelectronics, Rousset, France;* ²*Analog & Power Front-End Manufacturing, STMicroelectronics, Catania, Italy*

9:20 - 9:40

Segmented Centroid and Stress-buffered P-body Taps for Stable Multi-finger Power CMOS

JungHyun Oh^{1,2}, JungKyung Kim³, JaeHong Jeong³, Hoon Chang³, OhKyum Kwon³, SoYoung Kim⁴

¹*Department of Semiconductor and Display Engineering, Sungkyunkwan University, Suwon, Korea;* ²*Samsung Institute of Technology, Samsung Electronics, Yongin, Korea;* ³*Foundry Business, Samsung Electronics, Yongin, Korea;* ⁴*Department of Semiconductor Systems Engineering, College of Information and Communication Engineering, Sungkyunkwan University, Suwon, Korea*

9:40 - 10:00

Charge Field Modulation Mechanism and Its Experiments in SJ-Based SOI BCD process

Wentong Zhang¹, Jiangnan Mu¹, Teng Liu¹, Nailong He², Liqi An², Jingchuan Zhao², Sen Zhang², Ping Li³, Rongyao Ma³, Yongqiang Cai⁴, Ming Qiao¹, Zhaoji Li¹, Bo Zhang¹

¹*State Key Laboratory of Electronic, Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu, China;* ²*Technology Development Department, CSMC Technologies, Wuxi, China;* ³*China Resources Microelectronics, Chongqing, China;* ⁴*Beijing Normal University, Beijing, China*

10:00 - 10:20

High Performance Producible 90nm CFP LDMOS with a Secondary DPN-ISSG FP

Shaoxin Yu¹, Rongsheng Chen¹, Bo Wang², Xiaolong Zhao², Qishun Yao², Yan Jin²

¹*School of Microelectronics, South China University of Technology, Guangzhou, China;* ²*R&D department, Runpeng Semiconductor Technology, Shenzhen, China*

10:20 - 10:50 3F A1/A2 Room and Foyer (Exhibition Area)

Coffee Break

10:50 - 12:30 4F Main Hall

ICD: Power IC Design

Chairs: Jingshu Yu (*Intel, USA*)

Wei-Jia Zhang (*Analog Device, USA*)

10:50 - 11:10 **A Monolithic GaN IC with Temperature Compensated Active Clamp Driver and Short Circuit Protection for Wide Power Supply Range**

Yi Lu¹, Xin Ming^{1,2,3}, Yao Qin¹, Lin-min Chen¹, Chun-wang Zhuang¹, Xin-ce Gong¹, Wen-xi Lu¹, Bo Zhang¹

¹State Key Laboratory of Electronic, Thin Films and Integrated Devices, UESTC, Chengdu, China;

²Shenzhen Institute for Advanced Study, UESTC, Shenzhen, China; ³Institute of Electronic and Information of UESTC in Guangdong, Dongguan, China

11:10 - 11:30 **Dynamic Reliability of IC-Interface GaN HEMTs Demonstrated under Ultra-Fast (ns), High-Frequency (MHz) Gate Overvoltage Stress (>30 V)**

Bixuan Wang¹, Qihao Song¹, Kalparupa Mukherjee², Loizos Efthymiou², Daniel Popa², Giorgia Longobardi², Dong Dong¹, Florin Udrea², Yuhao Zhang³

¹Center for Power Electronics Systems (CPES), Virginia Tech, Blacksburg, USA; ²Cambridge GaN

Devices, Cambridge, UK; ³Department of Electrical & Electronic Engineering, The University of Hong Kong, Hong Kong, China

11:30 - 11:50 **12-V Tolerant Power-Rail ESD Clamp Circuit for Monolithic GaN-on-Silicon Integrated Circuits**

Chao-Yang Ke, Ming-Dou Ker

Institute of Electronics, National Yang Ming Chiao Tung University, Hsinchu, Taiwan

11:50 - 12:10 **A Self-Powered Gate Driving Scheme Enabled by the GaN/SiC Cascode Power Device**

Ji Shu¹, Jiahui Sun^{1,2}, Mian Tao³, Shi-Wei Ricky Lee³, Kevin J. Chen¹

¹Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong, China; ²College of Electrical Engineering, Zhejiang University,

Hangzhou, China; ³EPACK Lab, The Hong Kong University of Science and Technology, Hong Kong, China

12:10 - 12:30 **Closed-Loop Active Gate Driver IC With Gate Current Control When Collector Current Equals Load Current**

Yaogan Liang, Yohei Sukita, Michihiro Ide, Makoto Takamiya

The University of Tokyo, Tokyo, Japan

12:30 - 14:00 2F Civic Hall

Lunch Break

14:00 - 15:20 4F Main Hall

GaN-2: GaN Power Device Reliability and Tests

Chairs: Oliver Hilt (FBH, Berlin, Germany)

Roy K.-Y. Wong (National Tsing Hua University, Taiwan)

14:00 - 14:20 **Dynamic Stability and Reliability of Multi-Kilovolt GaN Monolithic Bidirectional HEMT**

Yuan Qin¹, Yijin Guo¹, Matthew Porter¹, Ming Xiao³, Hehe Gong¹, Zineng Yang¹, Daniel Popa⁴, Loizos Efthymiou⁴, Kai Cheng⁵, Zhiqin Chu², Han Wang², Florin Udrea^{4,6}, Yuhao Zhang²

¹Center for Power Electronics Systems, Virginia Tech, Blacksburg, VA, USA; ²Department of Electrical and Electronic Engineering, University of Hong Kong, Hong Kong, China; ³Xidian University, Xi'an, China; ⁴Cambridge GaN Devices, Cambridge, UK; ⁵Enkris Semiconductor, Suzhou, China; ⁶University of Cambridge, Cambridge, UK

14:20 - 14:40 **Verification of p-GaN Gate Lifetime Models through Wide Time-scale (μ s- 10^7 s) Measurement**

Sijiang Wu¹, Siyuan Ye¹, Jinjin Tang¹, Junting Chen¹, Shanshan Wang¹, Junlei Zhao¹, Zuoheng Jiang¹, Haohao Chen¹, Zheyang Zheng², Jun Ma¹, Mengyuan Hua¹

¹Department of Electronic and Electrical Engineering, Southern University of Science and Technology, Shenzhen, China; ²School of Microelectronics, University of Science and Technology of China, Hefei, China

14:40 - 15:00 **Ultrafast Junction Temperature Mapping During Surge Current Transient and Thermal Management in Vertical GaN PiN Diode**

Jiahong Du¹, Haobin Lin², Dazhi Hou², Shibing Long¹, Shu Yang¹

¹School of Microelectronics; ²Department of Physics, University of Science and Technology of China, China

15:00 - 15:20 **Mechanism of Leakage Current Degradation in p-GaN Gate HEMTs under Gamma Irradiation**

Zhao Wang¹, Qingchen Jiang¹, Shenghuai Liu¹, Xin Zhou¹, Huan Gao¹, Qi Zhou¹, Zhao Qi¹, Ming Qiao^{1,2}, Bo Zhang¹

¹State Key Laboratory of Electronic, Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu, China; ²Shenzhen Institute for Advanced Study, University of Electronic Science and Technology of China, Shenzhen, China

15:20 - 15:40 3F A1/A2 Room and Foyer (Exhibition Area)

Coffee Break

LVT-P: Low Voltage Power Devices 2 (Poster Session)

A Novel Split Contact Field Plate LDMOS with a Floating Gate for Hot Carrier Degradation Improvement

Qiao Teng¹, Yongyu Wu^{1,3}, Kai Xu^{1,2}, Dawei Gao¹

¹College of Integrated Circuits, Zhejiang University, Hangzhou, China; ²ZJU-Hangzhou Global Scientific and Technological Innovation Center, Zhejiang University, Hangzhou, China;

³Zhejiang ICsprout Semiconductor, Hangzhou, China

Novel Optimization Method of Multi-Devices using TCAD Driven Machine Learning in BCD Process

Junhyeok Kim¹, Kyuyeop Lee¹, Yunjun Nam¹, Joohyung Yoo¹, Juwon Park², Dawon Jeong¹, Jaehyun Yoo¹, Yonghee Park¹, Dae Sin Kim¹

¹CSE team, Samsung Electronics, Hwasung-Si, Korea; ²PA4 team, Samsung Electronics, Hwasung-Si, Korea

Chip Layout Optimization of Trench Length and the Upper Electrode Contact in Trench Field Plate MOSFET

Casey Clendennen¹, Tomoaki Shinoda¹, Shinpei Onishi¹, Hajime Kataoka¹, Masaki Nagata²

¹Device Development Dept., ROHM, Kyoto, Japan; ²Global IT Infrastructure Dept., ROHM, Kyoto, Japan

Irradiation Hardening of SGT Based on Combined IPO Structure and Mechanism Modeling of Leakage Current Optimization

Junyan Zhu¹, Haonan Liu¹, Jun Ye^{1,3}, Xuan Xiao^{3,4}, Ruihan Gao¹, Junfeng Yu¹, Xiaodong Yang¹, Zhuang Wang¹, Chunlei Wu¹, Weiye Mo³, Hongping Ma⁵, Qingchun Zhang⁵, Liang Li⁶, Qingdong Zhang⁷, Tao Wang⁷, Wei Huang², David Wei Zhang¹

¹Shanghai Institute of Intelligent Electronics & Systems, School of Microelectronics, Fudan University, Shanghai, China; ²School of Integrated Circuits, Jiangnan University, Wuxi, China;

³Wuxi China Resources Huajing Microelectronics, Wuxi, China; ⁴College of Physics, Sichuan University, Chengdu, China; ⁵School of Academy of Engineering & Technology, Fudan University, Shanghai, China; ⁶School of Electronic Information Engineering, Suzhou Vocational University, Suzhou, China; ⁷Wuxi Microelectronics Scientific and Research Center, Wuxi, China

Integrated Fast-Recovery SGT-SBR Devices with Majority Carrier Modulation during Wide Temperature Range

Jun Ye^{1,2}, Haonan Liu¹, Ruihan Gao¹, Xuan Xiao^{2,3}, Junyan Zhu¹, Weiye Mo², Yang Song², Xiaodong Yang¹, Zhuang Wang¹, Jiao Liang⁴, Hongping Ma⁴, Qingchun Zhang⁴, Wei Huang⁵, Chunlei Wu¹, David Wei Zhang¹

¹State Key Laboratory of ASIC and System, Shanghai Institute of Intelligent Electronics & Systems, School of Microelectronics, Fudan University, Shanghai, China; ²Wuxi China Resources Huajing Microelectronics, Wuxi, China; ³College of Physics, Sichuan University, Chengdu, China; ⁴Academy for Engineering & Technology, Fudan University, Shanghai, China; ⁵School of Integrated Circuits, Jiangnan University, Wuxi, China

BCD HVpMOS with Double-Functional-RESURF to Improve HCI Reliability

Tomohiro Imai¹, Atsushi Sakai¹, Zen Inoue²

¹Process Tech and PDK Department, Operations Engineering Division, Renesas Electronics, Ibaraki, Japan; ²MCU Device Technology Department, Device Technology Division, Renesas Electronics, Kumamoto, Japan

Novel Multistack Floating Field Plate MOSFET and Image Clustering-based Design Analysis

Hiro Gangi¹, Yasunori Taguchi¹, Kentaro Takagi¹, Kouta Nakata¹, Kairu Yoshida¹, Taichi Fukuda¹, Hiroki Nemoto¹, Shotaro Baba¹, Yusuke Kobayashi¹, Tomoaki Inokuchi¹, Tatsuya Nishiwaki², Kenya Kobayashi²

¹Corporate Research & Development Center, Toshiba, Kanagawa, Japan; ²Advanced Semiconductor Device Development Center, Toshiba Electronic Devices & Storage, Kanagawa, Japan

Design and Performance Enhancement of Integrated Schottky Contact in Low-Voltage LDMOS on 55nm BCD Platform

Dingxiang Ma¹, Yuanqing Ye², Yangjie Liao¹, Jiawei Wang¹, Fanyi Zeng², Bo Zhang¹, Ming Qiao^{1,2}

¹State Key Laboratory of Electronic, Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu, China; ²Shenzhen Institute for Advanced Study, University of Electronic Science and Technology of China, Shenzhen, China

High Reliability Tri-zone Heterogeneous Charge Balanced SJ-LDMOS with Novel Silicon Rich Oxide and Its Experimental Verification

Teng Liu^{1,2}, Hao Wang², Wentong Zhang¹, Nailong He², Shiyao Cai¹, Yuxiao Kun¹, Jiangnan Mu¹, Zhekai Hu¹, Ting Wang², Ziao Zhang², Liqi An², Yongshun Li², Huajun Jing², Liang Song², Sen Zhang², Yongsheng Sun³, Hao Fang³, Sheng Dong Hu⁴, Ming Qiao¹, Zhaoji Li¹, Bo Zhang¹

¹State Key Laboratory of Electronic, Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu, China; ²Technology Development Department, CSMC Technologies, Wuxi, China; ³Wuxi China Resources Microelectronics; ⁴Chongqing University, Chongqing, China

15:40 - 17:40 3F A3/A4 Room

ICD-P: Power IC Design 2 (Poster Session)

An On-Chip Tunable Negative Power Supply within SiC MOSFET Gate Driver for Spurious Conduction Suppression and Reliable Driving

Yun Dai, Zekun Zhou, Rongxing Lai, Zijun Zhou, Jiaying Mao, Bo Zhang

State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu, China

A Study on a 4H-SiC-Based ESD Protection Device with lower Operating Voltage Using an Additional PNP BJT Structure

U-Yeol Seo¹, Jae-Yoon Oh¹, Min-Seo Kim¹, Dong-Hyun Kim¹, Ji-Hye Yoo¹, Hee-Bae Lee², Seung-Hyun Kim², Kyu-Hyun Jung², Yong-Seo Koo³

¹Dept. Engineering of Foundry, Dankook University, Yongin, Korea; ²Tech Development Team3, DB HiTek, Bucheon, Korea; ³Dept. Engineering of Electronics and Electrical, Dankook University, Yongin, Korea

High Voltage Monolithic GaN Power IC with High Speed Low-power Consumption Level Shifter Circuit

Qianheng Dong¹, Jing Zhu², Yifei Zheng¹, Haoran Wang¹, Xiang Fan¹, Zihang Chen¹, Siyang Liu¹, Weifeng Sun¹, Kai Zhang³, Siyuan Yu⁴

¹National ASIC System Engineering Research Center, Southeast University, Nanjing, Jiangsu, China; ²Wuxi Institute of Integrated Circuit Technology, Southeast University, Wuxi, Jiangsu, China; ³Nanjing Electronic Devices Institute, Nanjing, Jiangsu, China; ⁴Wuxi Chipown Micro-electronics, Wuxi, China

A Dynamic Gate Driver with Auto-Patterning to Reduce Ringing and Switching Loss

Wentao Cui¹, Wei-Jia Zhang², Jingyuan Liang¹, Haruhiko Nishio³, Motomitsu Iwamoto³, Wai Tung Ng¹

¹The Edward S. Rogers Sr. Dept. of Electrical and Computer Engineering, University of Toronto, Toronto, ON, Canada; ²Dept. of Electrical and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong, China; ³Semiconductor Business Group, Fuji Electric, Matsumoto, Japan

LLC Resonant Converter Controller with Burst Mode Control and Soft-Start Function

Shuang-Quan Tsai¹, Wan-Chien Chen¹, Chang-Ching Tu², Yi-Kai Hsiao², Hao-Chung Kuo², Po-Hung Chen¹

¹Institute of Electronics, National Yang Ming Chiao Tung University, Hsinchu, Taiwan; ²Hon Hai Research Institute, Hsinchu, Taiwan

A High Precision and Robustness Isolated Analog Signal Sensing For Monitoring Power Stages

Yu-han Chen, Xin Ming, Yu-tong Wu, Tian-yi Sun, Jun-yu Chen, Zhuo Wang, Bo Zhang

State key Laboratory of Electronic, Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu, China

15:40 - 17:40 3F A3/A4 Room

GaN-P1: GaN Devices (Poster Session)

Dynamic Performance Analysis of GaN Digital Logic Gate Circuits for MHz-level Operation via CTL-based ICs Platform

Yang Jiang^{1,2}, Fangzhou Du¹, Ziyang Wang¹, Kangyao Wen¹, Mujun Li¹, Yifan Cui¹, Han Wang², Qing Wang¹, Hongyu Yu^{1,3}

¹School of Microelectronics, Southern University of Science and Technology, Shenzhen, China; ²Department of Electrical and Electronic Engineering, The University of Hong Kong, Pokfulam Road, Hong Kong; ³School of Integrated Circuit, Shenzhen Polytechnic University, Shenzhen, China

A Comprehensive Study on Device Reliability and Failure Mechanism of 650V p-GaN Gate HEMTs Under Long-Term HTRB Stress Beyond 150 ° C

Lei Tang¹, Jinggui Zhou¹, Binju Qiu¹, Huan Gao¹, Jianggen Zhu¹, Kuangli Chen¹, Ning Yang¹, Bo Zhang¹, Qi Zhou^{1,2}

¹School of Integrated Circuit Science and Engineering, University of Electronic Science and Technology of China, Chengdu, China; ²Institute of Electronic and Information Engineering, UESTC, Dongguan, China

Dependence of UIS Capability in GaN HEMTs on Substrate Bias and p-Gate Contacts

Wataru Saito, Shin-ichi Nishizawa

Research Institute for Applied Mechanics, Kyushu University, Fukuoka, Japan

Self-aligned p-GaN Gate Controlled Diodes With Tunable Forward Conduction/Reverse Blocking Properties For High Efficiency Buck Converter

Jinggui Zhou¹, Shuting Huang¹, Jianggen Zhu¹, Yuqi Liu¹, Enchuan Duan¹, Lei Tang¹, Wenzheng Liu¹, Xuan Li¹, Peng Luo³, Yong Liu³, Qi Zhou^{1,2}, Bo Zhang¹

¹School of Integrated Circuit Science and Engineering, University of Electronic Science and Technology of China, Chengdu, China; ²Institute of Electronic and Information Engineering, UESTC, Dongguan, China; ³Nanjing Dan Xi Technology, China

Impact of Substrate Termination on the Performances of Monolithic ESD Protection Circuit Using Bidirectional GaN HEMTs

Yanfeng Ma¹, Sheng Li¹, Hao Yan¹, Lixi Wang¹, Mingfei Li¹, Weihao Lu¹, Jie Ma¹, Ran Ye¹, Denggui Wang^{2,3}, Jianjun Zhou^{2,3}, Wangran Wu¹, Jiaying Wei¹, Long Zhang¹, Siyang Liu¹, Weifeng Sun¹

¹National ASIC System Engineering Research Center, Southeast University, Nanjing, China; ²State Key Laboratory of Wide-Bandgap Semiconductor Devices and Integrated Technology & ³Nanjing Electronic Devices Institute, Nanjing, China

High-V_{th} E-Mode PIN-Gate GaN HEMT : Supporting Gate Drive Voltages >12 V

Mao Jia, Bin Hou, Ling Yang, Xuefeng Zheng, Xiaohua Ma, Yue Hao

National Engineering Research Center of Wide Band-gap Semiconductor, Xidian University, Xi'an, China

Monolithic Heterogeneous Integration of 6-Inch GaN/Si CMOS 1P2M Process on Si (111) Substrate and Platformed Devices

Wenzhang Du¹, Hanzhao He¹, Xiaojun Fu⁷, Wenqi Fan¹, Junyan Zhu¹, Junfeng Yu¹, Xiaodong Yang¹, Haonan Liu¹, Zhuang Wang¹, Ruihan Gao¹, Jiao Liang³, Hongping Ma³, Qinchun Zhang³, Wang Ma⁴, Li Yuan⁴, Zhaojun Liu⁵, Guangsheng Zhang⁷, Chen Qian⁷, Yuan Wang⁸, Yue-Chan Kong⁸, HaiOu Li⁹, Tao Wang⁶, Liang Li¹⁰, Yuan-Yang Xia¹¹, Yi-Heng Li¹¹, Ting Gang Zhu¹¹, Shujun Cai⁶, Wei Huang², David Wei Zhang¹

¹School of Microelectronics, Fudan University, Shanghai, China; ²School of Integrated Circuits, Jiangnan University, Wuxi, China; ³School of Academy for Engineering & Technology, Fudan University, Shanghai, China; ⁴Genettice, Qingdao, China; ⁵Southern University of Science and Technology, Shenzhen, China; ⁶National Key Laboratory of Integrated Circuits and Microsystems, Wuxi, China; ⁷National Key Laboratory of Integrated Circuits and Microsystems, Chongqing, China; ⁸Nanjing Electronic Devices Institute, Nanjing, China; ⁹Guilin University of Electronic Technology, Guilin, China; ¹⁰School of Electronic Information Engineering, Suzhou Vocational University, Suzhou, China; ¹¹CorEnergy Semiconductor, Zhangjiagang, China

Enhanced Irradiation Capability in AlGaIn/GaN p-GaN-Hybrid Anode Power Diodes via Structural Hardening Design

Feng Zhou^{1,2}, Tianyang Zhou¹, Tianqi Wang³, Peipei Hu⁴, Pengfei Zhai⁴, Jie Liu⁴, Zhichao Wei⁵, Yuanyang Xia⁶, Leke Wu⁶, Ke Wang⁶, Yiheng Li⁶, Tinggang Zhu⁶, Weizong Xu¹, Dunjun Chen¹, Rong Zhang¹, Hai Lu¹

¹School of Electronic Science and Engineering, Nanjing University, Nanjing, China; ²Shenzhen Research Institute of Nanjing University, Shenzhen, China; ³Space Environment Simulation Research Infrastructure (SESRI), Harbin Institute of Technology, Harbin, China; ⁴Institute of Modern Physics, Chinese Academy of Sciences, Lanzhou, China; ⁵China Academy of Space Technology, Beijing, China; ⁶CorEnergy Semiconductor, Suzhou, China

Physical Model of Trapping-Induced Dynamic Degradation in GaN HEMT

Chih-Kai Chang¹, Chao-Ta Fan¹, Pao-Tin Lin¹, Yen-Chieh Huang¹, Po-Chin Peng², Cheng Chun Huang², Ming-Cheng Lin¹

¹Device Dynamics Lab Hsinchu, Taiwan; ²ANCORA Semiconductors, Taoyuan, Taiwan

Experiment and Simulation Study of Single-Event Burnout in GaN Event-Triggering HEMTs

Ruize Sun^{1,2}, Renjie Wu¹, Xiaoming Wang³, Yun Xia³, Chao Liu¹, Wanjun Chen^{1,2}, Bo Zhang¹

¹State Key Laboratory of Electronic, Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu, China; ²Institute of Electronic and Information Engineering of UESTC in Guangdong, Dongguan, China; ³Shenzhen Pinghu Laboratory, Shenzhen, China

Comparison of Total Ionizing Dose Effects in GaN HEMTs with p-GaN Gate Structure and Cascode Configuration

Chen-Yu Yang¹, Der-Sheng Chao², Jenq-Horng Liang^{1,3}

¹Department of Engineering and System Science (ESS), National Tsing-Hua University, Hsinchu, Taiwan; ²Nuclear Science and Technology Development Center, National Tsing-Hua University, Hsinchu, Taiwan; ³Institute of Nuclear Engineering and Science, National Tsing-Hua University, Hsinchu, Taiwan

Reverse Recovery Loss in Monolithic GaN Half-Bridge Chip with P-N Junction Isolation

Mingfei Li¹, Sheng Li¹, Fenglei Song¹, Yanfeng Ma¹, Weihao Lu¹, Jianjun Zhou², Denggui Wang², Jie Ma¹, Ran Ye¹, Jiaying Wei¹, Long Zhang¹, Siyang Liu¹, Weifeng Sun¹

¹National ASIC System Engineering Research Center, Southeast University, Nanjing, China; ²Nanjing Electronic Devices Institute, Nanjing, China

Heavy-Ion Radiation-Induced Dynamic On-Resistance Degradation for P-GaN Gate HEMTs

Huan Gao¹, Xin Zhou¹, Zhao Wang¹, Wen Yang², Qi Zhou¹, Bo Zhang¹

¹University of Electronic Science and Technology of China (UESTC), Cheng Du, China; ²South China University of Technology (SCUT), Guang Zhou, China

Suppressed Substrate-Coupled Cross-Talk Effects in GaN-on-Sapphire Platform Under High-Temperature and High-Voltage Applications

Junsong Jiang¹, Bomin Jiang², Zhanfei Han³, Yang Zhang¹, Mengdie Zhang¹, Xingang Ren¹, Xi Tang¹, Xiangdong Li³, Shu Yang², Jincheng Zhang³

¹School of Electronic and Information Engineering and Institute of Physical Science and Information Technology, Anhui University, Hefei, China; ²School of Microelectronics, University of Science and Technology of China, Hefei, China; ³Guangzhou Wide Bandgap Semiconductor Innovation Center, Guangzhou Institute of Technology, Xidian University, Guangzhou, China

On the Rational Extraction of the Channel Mobility of Schottky-Type p-GaN Gate Power HEMTs

Chi Wang¹, Zhisheng Nie¹, Hao Zhang¹, Yifang Zhang¹, Li Zhang², Mengyuan Hua³, Shibing Long¹, Zheyang Zheng¹

¹School of Microelectronics, University of Science and Technology of China, Hefei, China; ²Silergy, Hong Kong, China; ³Southern University of Science and Technology, Shenzhen, China

A P-Channel GaN Insulated Gate Bipolar Transistor with Outstanding Current Capability

Mengyao Zhao¹, Jie Ma¹, Tianchun Nie¹, Qiwei Peng¹, Denggui Wang², Jianjun Zhou², Sheng Li¹, Jiaying Wei¹, Siyang Liu¹, Long Zhang¹, Weifeng Sun¹

¹*School of Integrated Circuits, Southeast University, Nanjing, China;* ²*Nanjing Electronic Devices Institute, Nanjing, China*

Engineering Extrinsic Resistance of E-Mode GaN p-FET towards Enhanced Current Density

Jialin Duan¹, Jingjing Yu¹, Teng Li¹, Hengyuan Qi¹, Sihang Liu¹, Yunhong Lao¹, Maojun Wang¹, Junchun Bai³, Bin Cheng³, Jinyan Wang¹, Bo Shen², Jin Wei¹

¹*School of Integrated Circuits, Peking University, Beijing, China;* ²*School of Physics, Peking University, Beijing, China;* ³*Xingang Semiconductor, Xuzhou, China.*

Improved Normally-off 1200 V GaN-on-Si MOS-HEMT with Novel AlGaN Back Barrier

Cédric Masante, Stéphane Bécu, Blend Mohamad, Aurélien Olivier, Florent Gréco, Rémi Riat, Simona Torrenco, Johnny Amiran, Romain Laviéville, Arnaud Anotta, Etienne Nowak

Univ. Grenoble Alpes, CEA, Leti, Grenoble, France

Investigation of Dynamic R_{ON} in p-GaN Gate HEMTs under Steady-State Soft-Switching: Roles of OFF-State Trapping and Hole Injections

Hongkeng Zhu, Elison Matioli

Power and Wide-Band-Gap Electronics Research Laboratory (POWERlab), Institute of Electrical and Micro Engineering, École Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland

Demonstration of 3300-V GaN HEMTs on 6-inch Sapphire for Medium-Voltage Applications: A Cost Effective and High-Performance Solution

Junbo Wang¹, Xiangdong Li^{1,2}, Jian Ji¹, Lili Zhai¹, Lu Yu¹, Zhanfei Han¹, Tao Zhang^{1,2}, Xi Jiang^{1,2}, Song Yuan^{1,2}, Long Chen³, Lezi Wang³, Zilan Li³, Weitao Yang⁴, Chao Sheng⁴, Shuzhen You^{1,2}, Yue Hao^{1,2}, Jincheng Zhang^{1,2}

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Dynamic Threshold Voltage Extraction for GaN HEMT via a Source-Series-Connected Capacitor

Wenkang Ji¹, Ying Wang¹, Zhixing Zhao², Zilin Wu¹, Haifeng Zhan², Lekang Fan¹, Zesen Chen¹, Zuoran Luo¹, Tian Luo¹, Qianshu Wu¹, Jinwei Zhang¹, Zixin Wang¹, Yang Liu¹

¹*School of Electronics and Information Technology, Sun Yat-Sen University, Guangzhou, China;* ²*Hunan GiantSun Power Electronics, Chenzhou, China*

A > 10 kV/2.1 GW/cm² AlGaIn/GaN SBD with Current-Collapse Suppression via in-situ NH₃ Plasma Treated GaN Passivation

Jiahao Chen¹, Ruowei Liu¹, Tao Zhang¹, Shengrui Xu¹, Huake Su¹, Jinfeng Zhang¹, Zeyang Ren¹, Xiangdong Li², Hongchang Tao¹, Yue Hao¹, Jincheng Zhang¹

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Realization of High-Voltage Depletion-mode HEMTs with Tunable Threshold Voltage on a Standard Enhancement-mode GaN Platform

Fengping Lin¹, Xiaoyu Liu¹, Zhiwen Dong², Junsong Jiang¹, Suxia Guo¹, Changhui Zhao¹, Zhaofu Zhang³, Baikui Li⁴, Gaofei Tang², Xi Tang¹

¹Institute of Physical Science and Information Technology, Anhui University, Hefei, China; ²CloudSemi Technology, Hangzhou, China; ³The Institute of Technological Sciences, Wuhan University, Wuhan, China; ⁴College of Physics and Optoelectronic Engineering, Shenzhen University, Shenzhen, China

Dynamic On-Resistance Degradation in E-mode GaN HEMTs Under Over-Voltage Hard Switching Stress: Insight of Physical Space and Energy Levels

Haoran Wang¹, Po-Yen Huang², Wei-Ting Hsu¹, Shawn S. H. Hsu^{1,2}, Roy K.-Y. Wong^{1,2}

¹Institute of Electronics Engineering, National Tsing Hua University, Hsinchu, Taiwan; ²College of Semiconductor Research, National Tsing Hua University, Hsinchu, Taiwan

High-performance InAlN/GaN HEMTs and Monolithically Integrated Inverters enabled by InAlO_xN_{1-x} Plasma-Induced-Oxidation Charge Trapping Layer

Fangzhou Du¹, Yang Jiang^{1,2}, Ziyang Wang¹, Kangyao Wen¹, Mujun Li¹, Xiaohui Wang¹, Yi Zhang^{1,2}, Chenkai Deng¹, Qing Wang¹, Hongyu Yu^{1,3}

¹School of Microelectronics, Southern University of Science and Technology, Shenzhen, China; ²Department of Electrical and Electronic Engineering, The University of Hong Kong, Pokfulam Road, Hong Kong; ³School of Integrated Circuit, Shenzhen Polytechnic University, Shenzhen, China

Dynamic Overvoltage and Energy Loss in p-GaN HEMTs under Ultraviolet Pulsed Laser-Induced Single Event Irradiation

Mai Zhang^{1,2}, Feng Zhou^{1,2}, Yijun Shi³, Zhengxiang Tang¹, Can Zou^{1,2}, Weizong Xu¹, Dong Zhou¹, Fangfang Ren¹, Dunjun Chen¹, Rong Zhang¹, Hai Lu¹

¹School of Electronic Science and Engineering, Nanjing University, Nanjing, China; ²Shenzhen Research Institute of Nanjing University, Shenzhen, China; ³China Electronic Product Reliability and Environmental Testing Research Institute, Guangzhou, China

Enhanced Single-Event Hardness in GaN-on-Si HEMT With Gate-Junction Termination Extension

Xuan Xie, Minze Wang, Ziang Wang, Zhi Wang, Chenyue Chu, Guangwei Xu, Shibing Long, Shu Yang

School of Microelectronics, University of Science and Technology of China, Hefei, China

Demonstration of High Voltage (>2000V) AlGaIn/GaN Schottky Barrier Diode with p-GaN Anode Edge Termination and Cathode-connected p-GaN Islands for Enhanced Dynamic R_{ON} Stability

Hung-Chun Chen¹, Pei-Jung Wang¹, Hung-Wei Chen², Tian-Li Wu^{1,2,3}

¹International College of Semiconductor Technology, National Yang Ming Chiao Tung University, Taiwan; ²Institute of Pioneer Semiconductor Innovation, National Yang Ming Chiao Tung University, Taiwan; ³Institute of Electronics and Department of Electronics and Electrical Engineering, National Yang Ming Chiao Tung University, Taiwan

Through-GaN-Via Design Rule Investigation of GaN Power HEMTs on Si Substrate

Longge Deng¹, Ji Shu¹, Jiahui Sun^{1,2}, Kevin J. Chen¹

¹Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong, China; ²College of Electrical Engineering, Zhejiang University, Hangzhou, China

Accurate Dynamic ON-resistance Characterization of Low-voltage GaN Power HEMTs

Yuwei Wu¹, Ji Shu¹, Jiahui Sun^{1,2}, Binghong Wang¹, Zongjie Zhou¹, Kevin J. Chen¹

¹Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong, China; ²College of Electrical Engineering, Zhejiang University, Hangzhou, China

High performance p-GaN gate HEMT with TiN_xO_y resistive field plate structure

Zhuocheng Wang¹, Wanjun Chen¹, Fangzhou Wang², Cheng Yu¹, Xiaochuan Deng¹, Ping Yu², Zheyu Huang¹, Yang Wang², HaiQiang Jia^{2,3}, Hong Chen³, Bo Zhang¹

¹State Key Laboratory of Electronic, Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu, China; ²Songshan Lake Materials Laboratory, Dongguan, China; ³Institute of Physics, China Academy of Sciences, Beijing, China

On the Impacts of Mobility Mismatching-Induced Asymmetric Rising and Falling Edges in GaN-based CMOS Circuits for Prospective Power Integration

Yang Zhang, Haoran Tao, Junchen Huang, Xiaomin Wang, Shibing Long, Zheyang Zheng

School of Microelectronics, University of Science and Technology of China, Hefei, China

Expanded Gate-Voltage Operating range of p-GaN gate HEMTs Operated in Synchronized Photonic-Electronic Driving (SPED) Scheme

Longge Deng, Haochen Zhang, Zheng Wu, Yan Cheng, Tao Chen, Kevin J. Chen

Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong, China

High I_{ON}/I_{OFF} Ratio > 10^5 Ag-Gated E-Mode GaN p-FETs Enabled by p^{++} -GaN Contact and Polarization-Enhanced AlN Layer

Zhiwei Sun^{1,2}, Hao Tian^{1,2}, Weisheng Wang^{1,2}, Xuanming Zhang^{1,2}, Maoqing Ling^{1,2}, Jie Zhang^{2,3}, Yinchao Zhao^{2,3}, Harm van Zalinge², Ivona Z. Mitrovic², Kain Lu Low^{1,2}, Sen Huang⁴, Wen Liu^{1,2},

¹School of Advanced Technology, Xi'an Jiaotong-Liverpool University, Suzhou, China;

²Department of Electrical Engineering and Electronics, University of Liverpool, Liverpool, UK;

³School of Chips, Entrepreneur College, Xi'an Jiaotong-Liverpool University, Suzhou, China;

⁴Institute of Microelectronics, University of Chinese Academy of Sciences, Beijing, China

Surge Current Operation of Power GaN HEMTs with p-GaN Gate under Positive Gate Voltage

Maximilian Goller, Madhu Lakshman Mysore, Dezhi Yang, Mohamed Alaluss, Josef Lutz, Thomas Basler

Chair of Power Electronics, University of Technology Chemnitz, Chemnitz, Germany

A Highly Linear 2-Transistor Monolithic Temperature Sensor Employing p-GaN HEMTs for GaN Power ICs

Fangqing Li^{1,2}, Yifan Dong^{1,2}, Xinyu Sun^{1,2}, Haodong Wang^{1,2}, Xin Chen², Yaozong Zhong², Hongwei Gao^{1,2}, Haoran Qie², Tengfei Li^{1,2}, Gaofei Zhi², Yu Zhou^{1,2}, Qian Sun^{1,2}, Hui Yang^{1,2}

¹School of Nano Technology and Nano Bionics, University of Science and Technology of China, Hefei, China; ²Key Laboratory of Semiconductor Display Materials and Chips, Suzhou Institute of Nano-Tech and Nano-Bionics, Chinese Academy of Sciences, Suzhou, China

Dual- vs. Single-Peak Transconductance Evolution in Schottky p-GaN Gate HEMTs: Influence of Partially and Fully Depleted p-GaN layer

Xuan Liu, Chao Feng, Yuhao Wang, Xinyue Dai, Zuoheng Jiang, Keping Wu, Jiawei Chen, Danfeng Mao, Rongxing Du, Xiaoping Wang, Haolin Hu, Wei Zeng, David Zhou, Yuxi Wan

Shenzhen Pinghu laboratory, Shenzhen, China

15:40 - 17:40 3F A3/A4 Room

GaN-P2: Vertical GaN Devices (Poster Session)

Enhancing Key Performance of Vertical p-NiO/n-GaN Heterojunction Diodes through Plasma Treatment and Oxygen Post-Annealing

Yeying Huang^{1,2}, Min Wang^{1,2}, Na Sun³, Renqiang Zhu⁴, Xiaohua Li¹, Jianbo Liang⁵, Jiandong Ye³, Chunfu Zhang⁶, Hezhou Liu^{1,2}, Junfa Mao², Xinke Liu^{1,2}

¹College of Materials Science and Engineering, Shenzhen University, Shenzhen, China; ²State Key Laboratory of Radio Frequency Heterogeneous Integration, Shenzhen University, Shenzhen, China; ³School of Electronic Science and Engineering, Nanjing University, Nanjing, China; ⁴Shenzhen Institute for Advanced Study, University of Electronic Science and Technology of China, Shenzhen, China; ⁵Graduate School of Engineering, Osaka Metropolitan University, Osaka, Japan; ⁶State Key Discipline Laboratory of Wide Band Gap Semiconductor Technology, Xidian University, Xi'an, China

Enhancing Key Performance of Vertical GaN MOS Capacitors through GaO_x Interface Technology

Jinpei Lin^{1,2}, Xinyi Pei³, Xiaohua Li¹, Haiwen Liu², Renqiang Zhu⁴, Chunfu Zhang⁵, Hsien-Chin Chiu⁶, Jianbo Liang⁷, Hezhou Liu^{1,2}, Junfa Mao², Xinke Liu^{1,2}

¹College of Materials Science and Engineering, Shenzhen University, Shenzhen, China; ²State Key Laboratory of Radio Frequency Heterogeneous Integration, Shenzhen University, Shenzhen, China; ³School of Electronic Science and Engineering, Nanjing University, Nanjing, China; ⁴Shenzhen Institute for Advanced Study, University of Electronic Science and Technology of China, Shenzhen, China; ⁵State Key Discipline Laboratory of Wide Band Gap Semiconductor Technology, Xidian University, Xi'an, China; ⁶Department of Electronic Engineering, Chang Gung University, Taoyuan, Taiwan; ⁷Graduate School of Engineering, Osaka Metropolitan University, Osaka, Japan

Analysis of Acceptor Activation and Lateral Diffusion of Channeled-implanted Mg Atoms in Vertical GaN Junction Barrier Schottky Diodes

Kazuki Kitagawa¹, Tsutomu Uesugi², Masahiro Horita¹, Tetsu Kachi², Jun Suda¹

¹Department of Electronics, Nagoya University, Nagoya, Japan; ²Institute of Materials and Systems for Sustainability (IMaSS), Nagoya University, Nagoya, Japan

1500 V GaN-on-Si Vertical Power MOSFETs: from quasi-vertical to fully-vertical topology

Yuchuan Ma^{1,2}, Hang Chen^{1,2}, Shuhui Zhang^{1,2}, Xiangyu Teng^{1,2}, Xiaoping Meng^{1,2}, Huantao Duan³, Bin Hu³, Huimei Ma³, Jianfei Shen³, Minghua Zhu³, Jin Rao³, Chao Liu^{1,2}

¹School of Integrated Circuits, Shandong University, Jinan, China; ²Shenzhen Research Institute of Shandong University, Shenzhen, China; ³Huawei Technologies, Huawei Base, Bantian, Longgang district Shenzhen, Guangdong, China

Low ON-Resistance Vertical GaN-on-GaN Trench MIS-FET With Small Temperature Dependence

Zaitian Han, Hao Zhang, Shibing Long, Shu Yang

School of Microelectronics, University of Science and Technology of China, Hefei, China

High-Gain/Low-V_f GaN Bipolar Junction Transistor based on Heterogeneous Integration Process for Bandgap Reference Application

Yukai Huang¹, Junfeng Yu¹, Junyan Zhu¹, Xiaodong Yang¹, Wenzhang Du¹, Jiao Liang³, Ruihan Gao¹, Chunlei Wu¹, Hongping Ma³, Qingchun Zhang³, Jun Tang⁴, Liang Li⁵, Wei Huang², David Wei Zhang¹

¹School of Microelectronics, Fudan University, Shanghai, China; ²School of Integrated Circuits, Jiangnan University, Wuxi, China; ³School of Academy of Engineering & Technology Fudan University, Shanghai, China; ⁴CEC Compound Semiconductor, Ningbo, China; ⁵School of Electronic Information Engineering, Suzhou Vocational University, Suzhou, China

8:40 - 10:20

4F Main Hall

SiC-4: Gallium Oxide and Diamond Devices

Chairs: Peter Losee (*Qorvo, USA*)

Hiroshi Kono (*Toshiba Electronic Devices & Storage, Japan*)

8:40 - 9:00

3 kV/2.9 m $\Omega \cdot \text{cm}^2$ β -Ga₂O₃ Vertical p–n Heterojunction Diodes with Helium-implanted Edge Termination and Oxygen Post Annealing

Jiajun Han^{1,2}, Na Sun³, Xinyi Pei³, Kangkai Fan², Yu Xu², Zihao Huang², Renqiang Zhu⁵, Nengjie Huo¹, Jingbo Li⁶, Junfa Mao⁴, Jiandong Ye³, Xinke Liu^{2,4}

¹College of Electronic Science and Engineering (Microelectronics College), South China Normal University, Foshan, China; ²College of Materials Science and Engineering, Shenzhen University, Shenzhen, China; ³School of Electronic Science and Engineering, Nanjing University, Nanjing, China; ⁴State Key Laboratory of Radio Frequency Heterogeneous Integration, Shenzhen University, Shenzhen, China; ⁵Shenzhen Institute for Advanced Study, University of Electronic Science and Technology of China, Shenzhen, China; ⁶College of Optical Science and Engineering, Zhejiang University, Hangzhou, China

9:00 - 9:20

3.9 kV Vertical β -Ga₂O₃ Hetero-Junction Diode With High-Temperature Operational Capability

Jiangbin Wan¹, Hengyu Wang¹, Haoyuan Cheng¹, Chi Zhang¹, Ce Wang¹, Tiancheng Tao¹, Zijian Hu¹, Junze Li¹, Han Wang¹, Haoyu Wang¹, Haidong Yan^{1,2}, Na Ren^{1,2}, Qing Guo¹, Kuang Sheng^{1,2}

¹College of Electrical Engineering, Zhejiang University, Hangzhou, China; ²ZJU-Hangzhou Global Scientific and Technological Innovation Center, Zhejiang University, Hangzhou, China

9:20 - 9:40

Enhancing Continuous Switching Stability of β -Ga₂O₃ SBDs through Epitaxial Surface Condition and Edge Termination Optimizations

Haoran Wang¹, Chi-Rui Hwang¹, Po-Yen Huang², Yeke Liu¹, Shawn S. H. Hsu^{1,2}, Roy K.-Y. Wong^{1,2}

¹Institute of Electronics Engineering, National Tsing Hua University, Hsinchu, Taiwan; ²College of Semiconductor Research, National Tsing Hua University, Hsinchu, Taiwan

9:40 - 10:00

1844 V β -Ga₂O₃ Trench-MOS Schottky Barrier Diodes with Improved Electric Field of 5.2 MV/cm

Akio Takatsuka¹, Hironobu Miyamoto¹, Tsunetoshi Maehara², Yosuke Fujiwara², Kohei Sasaki¹, Akito Kuramata¹

¹Novel Crystal Technology, Saitama, Japan; ²Phenitac Semiconductor, Okayama, Japan

10:00 - 10:20

Over 1kV deep depletion diamond MOSFET

Damien Michez^{1,2}, Juliette Letellier², Julien Pernot³, Ralph Makhoul², Nicolas Rouger²

¹DIAMFAB, Grenoble, France; ²LAPLACE, Université de Toulouse, CNRS, INPT, Toulouse, France;

³Institut Néel, Grenoble, France

10:20 - 10:50 3F A1/A2 Room and Foyer (Exhibition Area)

Coffee Break

10:50 - 12:30 4F Main Hall

SiC-2: Design Approaches and Physics for Reliability and Performance of SiC Devices

Chairs: Kung-Yen Lee (*National Taiwan University, Taiwan*)
Shinsuke Harada (*AIST, Japan*)

10:50 - 11:10 **Impact of Insulating Layer Design in the Termination Region of SiC Devices on H³TRB Test**

Kohei Ebihara, Hiroki Niwa, Yosuke Nakata, Toshikazu Tanioka, Takeshi Murakami, Katsuhiko Fujiyoshi, Shigeru Okimoto, Kenji Hatori, Katsutoshi Sugawara, Tatsuro Watahiki

Advanced Technology R&D Center, Mitsubishi Electric, Hyogo, Japan

11:10 - 11:30 **1 cm² Chip Size, 10 kV Rated 4H-SiC MOSFETs with Efficient Termination Design and State-of-the-Art Device Performance**

Lingxu Kong^{1,3}, Sizhe Chen², Na Ren^{1,3}, Manyi Ji^{1,3}, Ce Wang¹, Yanjun Li³, Hongyi Xu³, Zheng Liu¹, Xiuyan Lin⁴, Xueqian Zhong², Wei Chen^{2,4}, Haitao Huang², Yongxi Zhang^{2,4}, Kuang Sheng^{1,3}

¹College of Electrical Engineering, Zhejiang University, Hangzhou, China; ²Inventchip Technology, Shanghai, China; ³ZJU-Hangzhou Global Scientific and Technology Innovation Center, Hangzhou, China; ⁴Zhejiang Inventchip Technology, Zhejiang, China

11:30 - 11:50 **Plasma Behavior of SiC MOSFETs with Engineered Substrates during Reverse Recovery**

Mohamed Alaluss¹, Madhu Lakshman Mysore¹, Clemens Herrmann¹, Sudhanshu Goel², Ahmed Elsayed², Thomas Basler¹

¹Chair of Power Electronics, Chemnitz University of Technology, Chemnitz, Germany; ²Robert Bosch GmbH, Reutlingen, Germany

11:50 - 12:10 **Dead Time Dependency of Bipolar Degradation in SiC MOSFETs**

Clemens Herrmann¹, Mengdi He¹, Mohamed Alaluss¹, Rudolf Elpelt², Larissa Wehrhahn-Kilian², Thomas Basler¹

¹Chair of Power Electronics, Chemnitz University of Technology, Chemnitz, Germany; ²Infineon Technologies AG, Erlangen, Germany

12:10 - 12:30 **Investigation of Optimum Gate Structures for 1.2-kV SiC MOSFETs by Analyzing Avalanche and Short-Circuit Withstanding Capabilities**

Kazuhiro Suzuki, Hiroshi Yano, Noriyuki Iwamuro

Graduate School of Pure and Applied Sciences, University of Tsukuba, Tsukuba, Japan

12:30 - 14:00 2F Civic Hall

Lunch Break

14:00 - 15:40 4F Main Hall

PK: Packaging Technologies

Chairs: Xavier Jorda (*IMB-CNM, Spain*)

Wei-Chung Lo (*Industrial Technology Research Institute, Taiwan*)

14:00 - 14:20 Low Loop Inductance in Power Semiconductor Module with Direct-Lead Bonding Busbar

Jiyeon Choi¹, Sihoon Choi², Jun Imaoka², Masayoshi Yamamoto²

¹Department of Electrical Engineering, Nagoya University, Nagoya, Japan; ²Institute of Materials and Systems for Sustainability (IMaSS), Nagoya University Nagoya, Japan

14:20 - 14:40 Packaging Technology and Evaluation Result of Ultra- Compact Double-Side Cooled Power Module

Yoshihiro Tateishi, Akira Kitamura, Keita Suzuki, Satoharu Tanai, Tetsuo Endoh, Yoshikazu Takahashi

Center for Innovative Integrated Electronic Systems, Tohoku University, Sendai, Japan

14:40 - 15:00 SiC MOSFET Chip Embedded Switching-Cell for Multilevel Converters

Mariana Raya¹, Emma Solà¹, Miquel Vellvehi¹, Xavier Perpiñà¹, Philippe Lasserre², Sergio Busquets-Monge³, Xavier Jordà¹

¹Power Devices and Systems (PDS) Group, Institute of Microelectronics of Barcelona, IMB-CNM (CSIC), Barcelona, Spain; ²Deep Concept, Pau, France; ³Electronic Engineering Department, Polytechnic University of Catalonia (UPC), Barcelona, Spain

15:00 - 15:20 Impact of Cu Clip and Wire-Bonded Packaging on the Surge Current Capability of SiC MOSFETs in the Third Quadrant

Feilin Zheng¹, Binqi Liang¹, Chao Zheng², Xuebao Li¹, Zhibin Zhao¹, Xiang Cui¹

¹State Key Laboratory of Alternate Electrical Power System with Renewable Energy Sources, North China Electric Power University, Beijing, China; ²Beijing Institute of Smart Energy, Huairou Laboratory, Beijing, China

15:20 - 15:40 Stability Analysis based on a Virtual Twin of SiC Power MOSFET Module

Ivana Kovacevic-Badstuebner¹, Anja K. Brandl¹, Michel Nagel¹, Fernando Aguilar Vega², Bogdan Popescu³, Dan Popescu³, Ulrike Grossner¹

¹Advanced Power Semiconductor (APS) Laboratory, ETH Zurich, Zurich, Switzerland; ²R&D, Ingeteam, Zamudio, Spain; ³Infineon Technologies AG, Neubiberg, Germany

15:40 - 16:00 3F A1/A2 Room and Foyer (Exhibition Area)

Coffee Break

HV-P: High Voltage Devices (Poster Session)

Extreme optimization of 1200V SuperJunction IGBT, competing with SiC MOSFET

Masahiro Tanaka¹, Naoki Abe¹, Akio Nakagawa²

¹Nihon Synopsys G.K., Tokyo, Japan; ²Nakagawa Consulting Office LLC., Chigasaki, Japan

Low EMI Noise Superjunction MOSFET with an Ndot region in the P-pillar

Ping Li¹, Rongyao Ma¹, Xin Zhang¹, Daili Wang¹, Kaifeng Tang¹, Wei Zeng¹,
Wentong Zhang², Teng Liu²

¹China Resources Microelectronics (Chongqing), Chongqing, China; ²State Key Laboratory of Electronic, Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu, China

Improved short-circuit ruggedness in FS-IGBTs through optimized n+ emitter design

Kaname Mitsuzuka, Ryutaro Ishizaki, Tatsuya Naito, Yuichi Onozawa

Semiconductors Business Group, Fuji Electric, Matsumoto, Japan

Reduction of control delay in Single-back and Double-front Gate-controlled IGBT for high frequency applications

Takato Yamamoto¹, Yusuke Kobayashi¹, Munetoshi Fukui², Tomoko Matsudai³,
Ryohei Gejo³, Takuya Saraya², Kazuo Itou², Toshihiko Takakura², Shinichi Suzuki²,
Teruyuki Ohashi¹, Tatsunori Sakano¹, Tomoaki Inokuchi¹, Toshiro Hiramoto²

¹Corporate Research & Development Center, Toshiba, Kanagawa, Japan; ²Institute of Industrial Science, The University of Tokyo, Tokyo, Japan; ³Advanced Semiconductor Device Development Center, Toshiba Electronic Devices & Storage, Kanagawa, Japan

The Electrical Impact of Oxygen and Carbon Related Defect Profile in Electron Beam Irradiated MCZ/FZ Wafers

Kodai Ozawa, Sho Nakanishi, Hiroshi Inagawa

Power Device Technology Department, Renesas Electronics, Ibaraki, Japan

A Superjunction MOSFET with Self-adjustable Electron Path for Low Reverse Recovery Charge

Tongyang Wang¹, Zehong Li^{1,2}, Ziming Xia¹, Yige Zheng¹, Jingcheng Feng¹

¹State Key Laboratory of Electronic, Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu, China; ²Chongqing Institute of Microelectronics Industry Technology, University of Electronic Science and Technology of China, Chongqing, China

Fabrication and Optimization of 1550 V Semi-Superjunction MOSFET with Ultra-low Specific On-Resistance and Enhanced Switching Performance

Guoliang Yao¹, Ming Qiao^{1,2}, Bo Zhang¹

¹State Key Laboratory of Electronic, Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu, China; ²Shenzhen Institute for Advanced Study, University of Electronic Science and Technology of China, Shenzhen, China

Thermal Analysis of Current Crowding in IGBTs under Stressful Operation in Resonant Converters

Conrad Ferrer¹, Miquel Vellvehi¹, Xavier Jordà¹, Manuel Fernández², Sergio Llorente², Xavier Perpiñà¹

¹Power Devices and Systems (PDS) Group, Institute of Microelectronics of Barcelona, IMB-CNM (CSIC), Barcelona, Spain; ²BSH Home Appliances Group, Zaragoza, Spain

Intelligent Design of Superjunction Devices Based on Physics-informed Neural Network

Jing Chen^{1,3}, Huiyuan Li^{1,3}, Haiwei Tan^{1,3}, Zhekai Hu², Jiafei Yao^{1,3}, Ziwei Hu^{1,3}, Ping Li⁴, Rongyao Ma⁴, Wentong Zhang^{1,2}, Bo Zhang², Yufeng Guo^{1,3}

¹College of Integrated Circuit Science and Engineering, Nanjing University of Posts and Telecommunications, Nanjing, China; ²University of Electronic Science and Technology, Chengdu, China; ³National & Local Joint Engineering Laboratory for RF Integration and Micro-Packaging Technologies, Nanjing, China; ⁴China Resources Microelectronics, Chongqing, China

An improved TCAD simulation procedure for platinum-diffused silicon power diodes

Calvin Stephen^{1,2}, Sophie Ngo¹, Greca Jean-Charles¹, Luong Việt Phung², Christophe Raynaud², Dominique Planson²

¹STMicroelectronics, Discrete & Filter Division, Tours, France; ²Univ Lyon, INSA Lyon, Université Claude Bernard Lyon 1, Ecole Centrale de Lyon, CNRS, Ampère, Villeurbanne, France

16:00 - 18:00 3F A3/A4 Room

PK-P: Packaging Technologies 2 (Poster Session)

Thermal Management by Using Small-area Chips and AI-based Design Optimization in SiC Modules

Teruyuki Ohashi¹, Shun Takeda², Eitaro Miyake², Hiroshi Kono³, Tomohiro Iguchi⁴, Kazuya Kodani⁵, He Du¹, Yasunori Taguchi¹, Mitsuhiro Kimura¹, Hideyuki Nakagawa¹, Ryosuke Iijima¹

¹Corporate Research & Development Center, Toshiba, Kawasaki, Japan; ²Package & Test Technology Development Center, Toshiba Electronic Devices & Storage, Japan; ³Advanced Semiconductor Device Development Center, Toshiba Electronic Devices & Storage, Japan; ⁴Corporate Manufacturing Engineering Center, Toshiba, Japan; ⁵Infrastructure Systems Research and Development Center, Toshiba Infrastructure Systems & Solutions, Japan

A Novel High-Performance Double-Sided Cooling SiC Power Module Based on Cu Sintering

Haobin Chen¹, Haidong Yan^{1,2}, Kuang Sheng^{1,2}

¹College of Electrical Engineering, Zhejiang University, Hangzhou, China; ²Global Scientific and Technology Innovation Center, Zhejiang University, Hangzhou, China

Source Current Circulation Phenomenon and Suppression Method of High Voltage SiC Devices

Tang Xinling, Wang Jingfei, Wei Xiaoguang, Wang Yaohua, Chen Jingzhi, Du Yujie, Wang liang, Zhang Hao

Beijing Huairou laboratory, Beijing, China

Non-Intrusive Online Junction Temperature Monitoring in Si and SiC Power MOSFETs

Miquel Tutusaus¹, Xavier Perpiñà¹, Miquel Vellvehi¹, Manuel Fernández², Sergio Llorente², Xavier Jordà¹

¹Power Devices and Systems (PDS) Group, Institute of Microelectronics of Barcelona, IMB-CNM (CSIC), Barcelona, Spain; ²BSH Home Appliances Group, Zaragoza, Spain

Chip-level Interconnection Techniques for Chip Embedding Integration of SiC MOSFETs

Emma Solà¹, Mariana Raya¹, Philippe Lasserre², David Sánchez¹, José Rebollo¹, Miquel Vellvehi¹, Xavier Perpiñà¹, Xavier Jordà¹

¹Power Devices and Systems (PDS) Group, Institute of Microelectronics of Barcelona, IMB-CNM (CSIC), Barcelona, Spain; ²Deep Concept, Pau, France

A Novel Lifetime Prediction Method for Press Pack Devices Based on Fretting Wear

Wei Xiaoguang, Tang Xinling, Liu Jianhui, Wang Jingfei, Yu Kefan, Du Yujie

Beijing Huairou laboratory, Beijing, China

A GaN Power Module Using a Copper PCB with Integrated Liquid-Cooled Heat Exchanger

Jingyuan Liang¹, Xuan Wang¹, Xiaoyun Zhang¹, Chun Yin Au Yeung¹, Andrei Catuneanu², Matthew Birkett², Wai Tung Ng¹

¹The Edward S. Rogers Sr. Department of Electrical and Computer Engineering, University of Toronto, Toronto, Ontario, Canada; ²Dana Canada, Advanced Technology and Research, Oakville, Ontario, Canada

16:00 - 18:00 3F A3/A4 Room

SiC-P1: SiC Devices (Poster Session)

Study on Differences in Single-Event Leakage Current of Planar-Gate and Asymmetric Trench-Gate SiC MOSFETs

Xiaoping Dong^{1,2}, Mingmin Huang^{1,2}, Yao Ma^{1,2}, Zhimei Yang^{1,2}, Yun Li^{1,2}, Min Gong^{1,2}

¹College of Physics, Sichuan University, Chengdu, China; ²Key Laboratory of Radiation Physics and Technology, Ministry of Education, Sichuan University, Chengdu, China

Impact of Bulk Defects on Reliability and Noise in 1200V SiC DMOSFETs

Huamao Chen¹, Shih-Chiang Shen¹, Chih-Hung Yen¹, Ju-Cheng Lin¹, Chih-Ming Lai¹, Yu-Ting Chen²

¹Electronic and Optoelectronic System Research Laboratories, Industrial Technology Research Institute, Hsinchu, Taiwan; ²Electrical Measurement Laboratories, Taiwan Semiconductor Research Institute, Hsinchu, Taiwan

Short Circuit Protection of Parallel SiC MOSFET Modules Based on Electro-thermal Design with High-Temperature I-V Characteristics

Makiko Hirano, Kazuya Kodani, Akihisa Matsushita, Atsuhiko Kuzumaki

Corporate Research and Development Center, Toshiba, Tokyo, Japan

Study of a novel hybrid design with an IGBT and a SiC-MOSFET in a fast-switching ANPC topology

Alexander Philippou, Thorsten Arnold, Martin Weidl, Max Falkowski,
Franz-Josef Niedernostheide

Infineon Technologies AG, Neubiberg, Germany

Analysis on BV_{DSS} Outlier Chips and Screening Technology for 1.2 kV Automotive SiC MOSFETs

Jinying Yu, Jingjing Cui, Bao Hu, Jie Deng, Baocheng Yuan

Li Auto, Beijing, China

Influence of substrate and epi buffer on SiC bipolar degradation for different voltage classes at high current levels

Larissa Wehrhahn-Kilian¹, Paul Salmen², Michael Brambach¹

¹Infineon Technologies AG, Erlangen, Germany; ²Infineon Technologies AG, Warstein, Germany

Impact of the SiC MOSFET Body Diode in Heavy Ion-Induced Single-Event Damage

Leshan Qiu^{1,2}, Yun Bai¹, Jiale Wang^{1,2}, Yan Chen^{1,2}, Jieqin Ding³, Chengzhan Li³,
Xinyu Liu¹

¹Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China; ²School of Integrated Circuits, University of Chinese Academy of Sciences, Beijing, China; ³Zhuzhou CRRC Times Semiconductor, Zhuzhou, China

A Physics-Based Fast Electro-Thermal Coupling Model for Wide-Temperature-Range Junction Temperature Assessment in SiC MOSFETs

Cheng Zhang^{1,2}, Wenyu Lu^{1,2}, Xuetong Zhou^{1,2}, Xinhong Cheng^{1,2}, Li Zheng^{1,2}

¹The State Key Laboratory of Materials for Integrated Circuits, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences; ²The Center of Materials Science and Optoelectronics Engineering, University of Chinese Academy of Sciences, Beijing, China

An analysis of UIS failure mechanism of 4H-SiC MOSFET in transition region

Chen Yan^{1,2}, Bai Yun¹, Li Chengzhan³, Wang Antao^{1,2}, Qiu Leshan^{1,2}, Tian Xiaoli¹,
Tang Yidan¹, Wang Xinhua¹, Liu Xinyu¹

¹Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, China; ²University of Chinese Academy of Sciences, Beijing, China; ³Zhuzhou CRRC Times Semiconductor, Zhuzhou, China

Outperformance of Asymmetric 4H-SiC Superjunction Geometry Beyond the Optimal Limit of Symmetric Design

Daisuke Iizasa, Hiroaki Shiraga, Seigo Mori, Yuki Nakano

Silicon Carbide Advanced Devices Development Division, ROHM, Kyoto, Japan

Impact of V_{TH} instability in SiC for solid-state circuit breaker application

Enea Bianda¹, Gioele Gregis², Elena Mengotti¹, Gerd Schlottig¹, Luca Raciti²,
Thomas Masper²

¹ABB Corporate Research Center, Baden-Dättwil, Switzerland; ²ABB SpA, Bergamo, Italy

Measurement of Free-Carrier Density in a 1.2 kV SiC Schottky Diode under Overstress Conditions

Ferran Bonet, Oriol Aviñó, Xavier Jordà, Xavier Perpiñá

Power Devices and Systems (PDS) Group, Institute of Microelectronics of Barcelona, IMB-CNM (CSIC), Barcelona, Spain

Demonstration of 1100 V 600 A/cm² 4H-SiC Lateral IGBT with Field Limiting Rings Termination Design

Mengyao Zhao¹, Jie Ma¹, Tianchun Nie¹, Qiwei Peng¹, Haowei Chen², Runhua Huang², Yu Huang², Song Bai², Jiaying Wei¹, Siyang Liu¹, Long Zhang¹, Weifeng Sun¹

¹School of Integrated Circuits, Southeast University, Nanjing, China; ²Nanjing Electronic Devices Institute, Nanjing, China

A Study on Fault Prediction and Redundancy Control of Parallel SiC-MOSFETs

Naoki Takagi¹, Tetsuo Endoh¹, Yoshikazu Takahashi¹, Akira Tamakoshi², Takahiro Hanyu², Yoshitaka Iwaji³

¹Center for Innovative Integrated Electronic Systems, Tohoku University, Sendai, Japan;

²Laboratory for Brainware Systems, Research Institute of Electrical Communication, Tohoku University, Sendai, Japan; ³Department of Electrical and Electronic Engineering, Ibaraki University, Ibaraki, Japan

Dynamic Transconductance Extraction Method and Application in Medium-Voltage SiC Module

Jie Ren¹, Menghao Li¹, Sideng Hu¹, Naoto Fujishima², Haruhiko Nishio²

¹College of Electrical Engineering, Zhejiang University, Hangzhou, China; ²Semiconductors Business Group, Fuji Electric, Matsumoto, Japan

Negative Gate Bias Induced V_{th} instability in SiC MOSFET: Role of Body Diode Conduction

Peixuan Wang^{1,2}, Yunhong Lao¹, Meng Zhang², Youyi Yin¹, Hao Chang¹, Hengyuan Qi^{1,2}, Michael Lee³, Jack Chen³, Tony Chau³, Jin Wei¹

¹School of Integrated Circuits, Peking University, Beijing, China; ²College of Microelectronics, Beijing University of Technology, Beijing, China; ³Alpha Power Solutions, Shanghai, China

The Latest Fabrication and Experimental Results of 1.2 kV Split-Gate 4H-SiC MOSFET with P+ Buffer

Yuzhi Chen, Chi Li, Zedong Zheng

Department of Electrical Engineering, Tsinghua University, Beijing, China

Monolithic Integration of Lateral 4H-SiC MOSFET and Insulated-Gate Resistive Load with Improved Linearity and High-Temperature Stability

Cheng Sung¹, Pin-Shiuan Kuo², Yu-Sheng Hsiao¹, Wei-Cheng Lin², Surya Elangovan³, Chia-Lung Hung³, Yi-Kai Hsiao³, Hao-Chung Kuo^{1,3,5}, Chang-Ching Tu^{3,4}, Tian-Li Wu^{1,2,6}

¹Institute of Pioneer Semiconductor Innovation, National Yang Ming Chiao Tung University, Taiwan; ²International College of Semiconductor Technology, National Yang Ming Chiao Tung University, Taiwan; ³Semiconductor Research Center, Hon Hai Research Institute, Taiwan; ⁴Department of Electrical Engineering, National Central University, Taiwan; ⁵Department of Photonics, National Yang Ming Chiao Tung University, Taiwan; ⁶Institute of Electronics and Department of Electronics and Electrical Engineering, National Yang Ming Chiao Tung University, Taiwan

Investigation of Termination Soft Breakdown Mechanisms in 1700V-SiC MOSFETs Under HTRB with Different Temperatures

Wei-Chieh Hung¹, Hung-Ming Kuo¹, Ting-Chang Chang^{1,2}, Po-Yu Yen¹, Chun-Hung Chiang², Bo-Yu Chen¹

¹Department of Physics, National Sun Yat-sen University, Kaohsiung, Taiwan; ²College of Semiconductor and Advanced Technology Research, National Sun Yat-sen University, Kaohsiung, Taiwan

Application-relevant Measurement of the Input Capacitance of SiC Power MOSFETs

Michel Nagel, Anja K. Brandl, Manuel Belanche, Ivana Kovacevic-Badstuebner, Ulrike Grossner

Advanced Power Semiconductor (APS) Laboratory, ETH Zurich, Zurich, Switzerland

Effects of Proton Irradiation on SiC Power Devices with Various Edge Termination Structures

Sangyeob Kim¹, Jeongtae Kim^{2,4}, Dong-Seok Kim², Hyuncheol Bae³, Gyuhyeok Kang⁴, Ogyun Seok¹

¹School of Electrical and Electronic Engineering, Pusan National University, Busan, Korea; ²Korea Atomic Energy Research Institute, Gyeongju, Korea; ³Electronics and Telecommunications Research Institute, Daejeon, Korea; ⁴Department of Semiconductor System Engineering, Kumoh National Institute of Technology, Gumi, Korea

Data-Driven Multi-Objective Optimization of SiC Power MOSFETs

Anja K. Brandl¹, Ivana Kovacevic-Badstuebner¹, Bhagyalakshmi Kakarla¹, Roland Niemeier², Ulrike Grossner¹

¹Advanced Power Semiconductor Laboratory (APS), ETH Zurich, Zurich, Switzerland; ²Ansys Germany GmbH, Weimar, Germany

Reliability Testing of SiC MOSFETs in Different Power Cycling Operating Modes - Focusing on the Challenges of Body Diode Testing

Lukas Hein, Patrick Heimler, Georg Schubert, Josef Lutz, Thomas Basler

Chair of Power Electronics, Chemnitz University of Technology, Chemnitz, Germany

An In-Depth Investigation of Gate Ringing Induced by Total Ionizing Dose in SiC MOSFETs

Jiahao Hu, Xiaochuan Deng, Yinglun Wang, Tao Xu, Xuan Li, Bo Zhang

School of Integrated Circuit Science and Engineering, University of Electronic Science and Technology of China, Chengdu, China

Optimisation of the Fabrication of Sidewall-Implanted Trenches in a 3.3 kV SiC Semi-Superjunction Schottky Barrier Diode

Arne Benjamin Renz¹, Kyrylo Melnyk¹, Nikolaos Iosifidis¹, Richard Jefferies¹, Marco Zignale², Patrick Fiorenza², Luca Maresca³, Andrea Irace³, Fabrizio Roccaforte², Neophytos Lophitis⁴, Peter Michael Gammon¹, Marina Antoniou¹

¹School of Engineering, University of Warwick Coventry, UK; ²Istituto per la Microelettronica e Microsistemi – IMM-CNR Catania, Italy; ³Department of Electrical Engineering and Information Technologies, University of Naples Federico II, Naples, Italy; ⁴Faculty of Engineering and Technology, Cyprus University of Technology, Limassol, Cyprus

Novel 1.2kV 4H-SiC deep p-well one-channel MOSFET with asymmetric channel design

Skylar deBoera¹, Seung Yup Jang^{1,2}, Adam Morgan², Woongje Sung¹

¹College of Nanotechnology Science and Engineering, University at Albany, Albany, NY, USA; ²NoMIS Power, Albany, NY, USA

Comparative Analysis Between Monolithically Integrated 1.2kV Bi-Directional MOSFETs and Bi-Directional JBSFETs

Stephen A. Mancini¹, Daixin Chen², Seung Yup Jang¹, Andrew Binder³, Richard Floyd³, Robert Kaplar³, Jack Flicker³, Stan Atcitty³, Justin Lynch¹, Adam J. Morgan⁴, Xiaoqing Song², Woongje Sung¹

¹University at Albany, College of Nanotechnology Science and Engineering, Albany, NY, USA; ²University of Arkansas, Department of Electrical Engineering and Computer Science, Fayetteville, AR, USA; ³Sandia National Laboratories, Albuquerque, NM, USA; ⁴NoMIS Power, Albany, NY, USA

Comparative Performance Evaluation and Analysis of High Voltage Superjunction, Charge-Balanced, and Conventional 4H-SiC DMOSFETs at Cryogenic and High Temperatures

Zhaowen He¹, Reza. Ghandi², Collin W. Hitchcock², Stacey Kennerly², T. Paul Chow¹

¹Rensselaer Polytechnic Institute, Troy, New York, USA; ²GE Aerospace, Niskayuna, New York, USA

Investigations on SiC LIGBT with Floating Field-Limiting Rings and Injection Enhancement Effect

Moufu Kong¹, Hongfei Deng¹, Mingliang Yang¹, Yingzhi Luo¹, Zhaoyu Ai¹, Bingke Zhang²

¹State Key Laboratory of Electronic, Thin Films and Integrated Devices of China, University of Electronic Science and Technology of China, Chengdu, China; ²Power Device Research and Development Centre, Leshan Share Electronic, Leshan, China

Capacitance Degradation of SiC MOSFETs under Dynamic Reverse Bias Stress: Displacement Current-Induced Charge Injection and JFET Design Optimization

Zhaoxiang Wei, Zhaokuan Liu, Guozhi Zhen, Junhou Cao, Hao Fu, Jiaxing Wei, Siyang Liu, Weifeng Sun

National ASIC System Engineering Research Center, School of Integrated Circuits, Southeast University, Nanjing, China

16:00 - 18:00 3F A3/A4 Room

SiC-P2: Gallium Oxide Devices (Poster Session)

Enhancing the Performance and Reliability of Large-Area β -Ga₂O₃ Schottky Barrier Diodes via Two-Step Oxygen Annealing

Jinyang Liu, Yuanjie Ding, Qiuyan Li, Shu Yang, Zheyang Zheng, Guangwei Xu, Shibing Long

University of Science and Technology of China, Hefei, China

Kilovolt-Class β -Ga₂O₃ Multi-Fin-Channel Diodes with Ohmic-Contact Anode

Gaofu Guo^{1,2}, Xiaodong Zhang¹, Chunhong Zeng¹, Tiwei Chen¹, Dengrue Zhao^{1,2}, Zhili Zou¹, Zhucheng Li¹, Li Zhang¹, Zhongming Zeng¹, Xianqi Dai², Baoshun Zhang¹

¹Nanofabrication facility, Suzhou Institute of Nano-Tech and Nano-Bionics, Chinese Academy of Sciences (CAS), Suzhou, Jiangsu, China; ²School of Physics, Henan Normal University, Xinxiang, Henan, China

Investigation of β -Ga₂O₃ Power Diodes with Failure Voltage of 300 V under LET of 82 MeV·cm²/mg

Song He¹, Jinyang Liu¹, Guangwei Xu¹, Weibing Hao¹, Tianqi Wang², Xuanze Zhou¹, Shu Yang¹, Shibing Long¹

¹University of Science and Technology of China, Hefei, China; ²Harbin Institute of Technology, Harbin, China

Over 3 kV Vertical Mo/ β -Ga₂O₃ Trench-HJBS Diode with Low Turn-on Voltage of 0.66 V

Qiuyan Li, Jinyang Liu, Zhao Han, Weibing Hao, Guangwei Xu, Shibing Long

University of Science and Technology of China, Hefei, China

Monolithic Integrated β -Ga₂O₃ Inverters Based on Charge Trapping Layer E-mode MOSFETs

Mujun Li¹, Xiaohui Wang¹, Yang Jiang^{1,2}, Fangzhou Du¹, Haozhe Yu¹, Qing Wang¹, Hongyu Yu^{1,3}

¹School of Microelectronics, Southern University of Science and Technology, Shenzhen, China;

²Department of Electrical and Electronic Engineering, The University of Hong Kong, Pokfulam Road, Hong Kong; ³School of integrated Circuit, Shenzhen Polytechnic University, Shenzhen, China

Degradation Mechanisms of β -Ga₂O₃ SBD Associated with Proton Irradiation-Induced Defects

Wenzhang Du¹, Yuangang Wang⁷, Junfeng Yu¹, Junyan Zhu¹, Xinbo Zou³, Liang Li⁴, Debin Zhang⁵, Yiwu Qiu⁶, Xinjie Zhou⁶, Tao Wang⁶, Zhihong Feng⁷, Hongping Ma⁸, Qingchun Zhang⁸, Wei Huang², Chunlei Wu¹, David Wei Zhang¹

¹Shanghai Institute of Intelligent Electronics & Systems, School of Microelectronics, Fudan University, Shanghai, China; ²School of Integrated Circuits, Jiangnan University, Wuxi, China;

³School of Information Science and Technology (SIST), ShanghaiTech University, Shanghai, China ⁴School of Electronic Information Engineering, Suzhou Vocational University, Suzhou, China; ⁵Shanghai Institute of Space Power-Sources, Shanghai, China; ⁶Wuxi Microelectronics Scientific and Research Center, Wuxi, China; ⁷National Key Laboratory of Solid-State Microwave Devices and Circuits, Shijiazhuang, Hebei, China; ⁸School of Academy for Engineering & Technology, Fudan University, Shanghai, China

Comparative Study on Transient Thermal Resistance for β -Ga₂O₃ SBDs with Junction-Side Cooling Implementation

Shuhei Fukunaga¹, Tsuyoshi Funaki¹, Jun Arima², Minoru Fujita², Jun Hirabayashi²

¹Graduate school of Engineering, Osaka University, Osaka, Japan; ²Advanced Products Development Center Technology & IP HQ, TDK, Chiba, Japan

Self-Aligned Gate Technology for N-Ion-Implanted β -Ga₂O₃ UMOSFET

Xuanze Zhou, Qi Liu, Guangwei Xu, Shibing Long

University of Science and Technology of China, Hefei, China

High-Voltage Ga₂O₃ Vertical Schottky Barrier Diode With Suspended Field Plate Assisted Shallow Mesa Termination

Desen Chen¹, Xiaorui Xu¹, Yicong Deng¹, Xueli Han², Zhengbo Wang², Duanyang Chen², Hongji Qi²

¹College of Physics and Information Engineering, Fuzhou University, Fuzhou, China; ²Key Laboratory of Materials for High Power Laser, Shanghai Institute of Optics and Fine Mechanics, Chinese Academy of Sciences, Shanghai, China

Investigation of Oxygen Vacancies and Reverse Leakage Suppression in High-Breakdown Vertical Ga₂O₃/4H-SiC Schottky Rectifiers

Ji-Hyun Kim, Soo-Young Moon, Geon-Hee Lee, Tae-Hee Lee, Seung-Hyun Park, Sang-Mo Koo

Department of Electronic Materials Engineering, Kwangwoon University, Seoul, Korea

Switching Reliability of NiO/Ga₂O₃ Bipolar Junction Evaluated by a Circuit Method

Hehe Gong¹, Xin Yang¹, Zineng Yang¹, Yuan Qin², Jiandong Ye³, Yuhao Zhang¹

¹Department of Electrical and Electronic Engineering, The University of Hong Kong, Hong Kong, China; ²Center for Power Electronics Systems (CPES), Virginia Tech, Blacksburg, USA; ³School of Electronic Science and Engineering, Nanjing University, Nanjing, China

Monolithic Integration of Enhancement- and Depletion-mode MOSFETs Based on Heteroepitaxial ϵ -Ga₂O₃ for Power ICs

Shengheng Zhu, Linxuan Li, Tiecheng Luo, Weiqu Chen, Chenhong Huang, Xifu Chen, Zimin Chen, Yanli Pei, Gang Wang, Xing Lu

State Key Laboratory of Optoelectronic Materials and Technologies, School of Electronics and Information Technology, Sun Yat-sen University, Guangzhou, China

Reliability of β -Ga₂O₃ Schottky Barrier Diodes with a High Breakdown Voltage of 2.97 kV at 473 K

Guangwei Xu, Weibing Hao, Shibing Long

University of Science and Technology of China, Hefei, China

19:00 - 21:30 Hotel Nikko Kumamoto (Door Open 18:30)

Banquet

8:40 - 10:20 4F Main Hall

HV-2: Multi-Gate Technology and SJ Devices

Chairs: Ayanori Gatto (*Mitsubishi Electric, Japan*)
Craig Fisher (*Vishay, UK*)

8:40 - 9:00 **A New Dimension of Hybrid Switches: Dual-gate IGBT and SiC MOSFET With Coordinated Gate Control**

Roman Baburske, Alexander Philippou
Infineon Technologies AG, Neubiberg, Germany

9:00 - 9:20 **Negative Gate Capacitance-Free Split-Gate-Resistance-Separation CSTBT™ for Ultra-Low Switching Loss**

Kazuya Konishi, Koyo Matsuzaki, Kohei Onda, Kohei Sako, Shinya Soneda
Advanced Technology R&D Center, Mitsubishi Electric, Hyogo, Japan

9:20 - 9:40 **Carrier-extraction Mechanism for MOS-controllable Stored-carrier Diode (MOSD)**

Hiroshi Suzuki¹, Yujiro Takeuchi¹, Yusuke Takada¹, Takashi Hirao¹, Tsubasa Moritsuka², Masaki Shiraishi², Tetsuo Oda², Tomoyasu Furukawa²
¹Research & Development Group, Hitachi, Ibaraki, Japan; ²Minebea Power Semiconductor Device, Ibaraki, Japan

9:40 - 10:00 **Next-Generation Superjunction Power Device with Trench Sidewall Doping**

Chia Liang Liao^{1,3}, Lucio Renna², Voon Cheng Ngwan¹, Clelia Galati², Natalia Spinella², Giuseppe Longo², Francesco Patane², Gianfranco Di-Stefano¹, Jian Xin Zheng³, Ning Xiang³
¹STMicroelectronics, AMK, Singapore; ²STMicroelectronics, Catania, Italy; ³Singapore Institute of Technology, Singapore

10:00 - 10:20 **Switching Loss Reduction in Superjunction IGBTs via Analysis of Vertical Charge Imbalance**

Tomohiro Tamaki¹, Atsufumi Inoue¹, Shiro Hino¹, Kazuyasu Nishikawa¹, Makoto Hashimoto², Mitsuhisa Kawase², Yohei Sudo², Tsutomu Ogawa², Tatsuro Watahiki¹
¹Advanced Technology R&D Center, Mitsubishi Electric, Hyogo, Japan; ²Nisshinbo Micro Devices, Japan

10:20 - 10:50 3F A1/A2 Room and Foyer (Exhibition Area)

Coffee Break

10:50 - 12:30 4F Main Hall

SiC-3: Novel Devices and Ruggedness of SiC

Chairs: Cheng-Tyng Yen (*Fast SiC Semiconductor, Taiwan*)

Takaaki Tominaga (*Mitsubishi Electric, Japan*)

10:50 - 11:10 First Demonstration of SiC MOSFET with Monolithically Integrated Short-Circuit Protection

Shinichi Kimoto¹, Tatsunori Sakano², Ryosuke Iijima², Mitsuo Okamoto¹

¹*Advanced Power Electronics Research Center, National Institute of Advanced Industrial Science and Technology, Tsukuba, Japan;* ²*Corporate Research & Development Center, Toshiba, Kanagawa, Japan*

11:10 - 11:30 Monolithic SiC Smart Power IC with Over-Temperature Protection

Mitsuo Okamoto, Atsushi Yao, Hiroshi Sato

Advanced Power Electronics Research Center, National Institute of Advanced Industrial Science and Technology, Tsukuba, Japan

11:30 - 11:50 Experimental Demonstration and Analysis of 4.5kV Bidirectional Superjunction Power DMOSFETs in 4H-SiC

Zhaowen He¹, Reza Ghandi², Collin W. Hitchcock², Stacey Kennerly², T. Paul Chow¹

¹*Rensselaer Polytechnic Institute, New York, USA;* ²*GE Aerospace, New York, USA*

11:50 - 12:10 Impact of bottom p-well grounding resistance on unclamped inductive switching ruggedness of SiC trench MOSFETs

Katsuhisa Tanaka¹, Yuji Kusumoto¹, Hideyuki Hasegawa¹, Hiroshi Kono¹, Kenya Sano²

¹*Advanced Semiconductor Device Development Center, Toshiba Electronic Devices & Storage, Hyogo, Japan;* ²*Semiconductor Division, Toshiba Electronic Devices & Storage, Hyogo, Japan*

12:10 - 12:30 The Accurate AC BTI Prediction of SiC Power MOSFETs by Comprehensive Understanding of Physical Mechanism Basic Vth Instability Phenomena

Tetsuya Yoshida¹, Katsumi Eikyu¹, Keiichi Maekawa¹, Hideki Aono¹, Tsunenobu Kimoto²

¹*Renesas Electronics, Ibaraki, Japan;* ²*Department of Electronic Science and Engineering, Kyoto University, Kyoto, Japan*

12:30 - 14:00 2F Civic Hall

Lunch Break

14:00 - 15:20 4F Main Hall

GaN-3: Novel GaN Power Device and Technologies 2

Chairs: Dong Seup Lee (*Texas Instruments, USA*)

Hiroyuki Handa (*Panasonic Holdings, Japan*)

14:00 - 14:20 **A Hybrid-Source Double-Channel p-GaN Gate AlGaIn/GaN HEMT Featuring Suppression of Buffer Trapping Effects on Both Forward and Reverse Conductions**

Xiaotian Tang^{1,2}, Zhongchen Ji^{1,2}, Qimeng Jiang^{1,2}, Sen Huang^{1,2}, Xinguo Gao¹,
Ke Wei^{1,2}, Xinhua Wang^{1,2}, Xinyu Liu^{1,2}

¹*Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, China;* ²*University of Chinese Academy of Sciences, Beijing, China*

14:20 - 14:40 **p-GaN Gate HEMT with the Buffer Hole Compensation Layer for Achieving Repetitive Avalanche-like Breakdown Capability**

Cheng Yu¹, Wanjun Chen¹, Fangzhou Wang², Zhuocheng Wang¹, Xiaochuan Deng¹,
Guojian Ding², Zheyu Huang¹, Yang Wang², Haiqiang Jia^{2,3}, Hong Chen³, Bo Zhang¹

¹*State Key Laboratory of Electronic, Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu, China;* ²*Songshan Lake Materials Laboratory, Dongguan, China;* ³*Institute of Physics, China Academy of Sciences, Beijing, China*

14:40 - 15:00 **Vth Adjustable p-Channel GaN FinFET For Complementary Logic Integration**

Maolin Pan¹, Hai Huang¹, Xin Hu¹, Yifei Zhao¹, Yinnan Yang¹, Saisheng Xu¹, Min Xu^{1,2}

¹*State Key Laboratory of ASIC and System, Shanghai Institute of Intelligent Electronics & Systems, School of Microelectronics, Fudan University, Shanghai, China;* ²*Shanghai Integrated Circuit Manufacturing Innovation Center, Shanghai, China*

15:00 - 15:20 **GaN/SiC-based Polarization Superjunction Hybrid HEMTs (PSJ-hyHEMTs) on Vicinal Off-angle SiC**

Akira Nakajima, Hirohisa Hirai, Yoshinao Miura, Kazutoshi Kojima, Tomohisa Kato,
Shinsuke Harada

Advanced Power Electronics Research Center, National Institute of Advanced Industrial Science and Technology, Tsukuba, Japan

15:20 - 15:50 4F Main Hall

Closing Session

Charitat Award and Best Poster Award

Ichiro Omura, General Chair

Yuichi Onozawa, Technical Program Committee Chair

Closing Remarks

Ichiro Omura, General Chair

ISPSD 2026 Announcement

David Sheridan, General Chair of ISPSD 2026 (*Alpha & Omega Semiconductor, USA*)

Sameh Khalil, Technical Program Committee Chair of ISPSD 2026
(*Infineon Technologies, USA*)

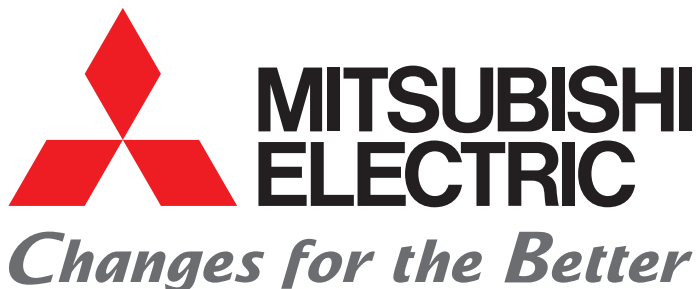
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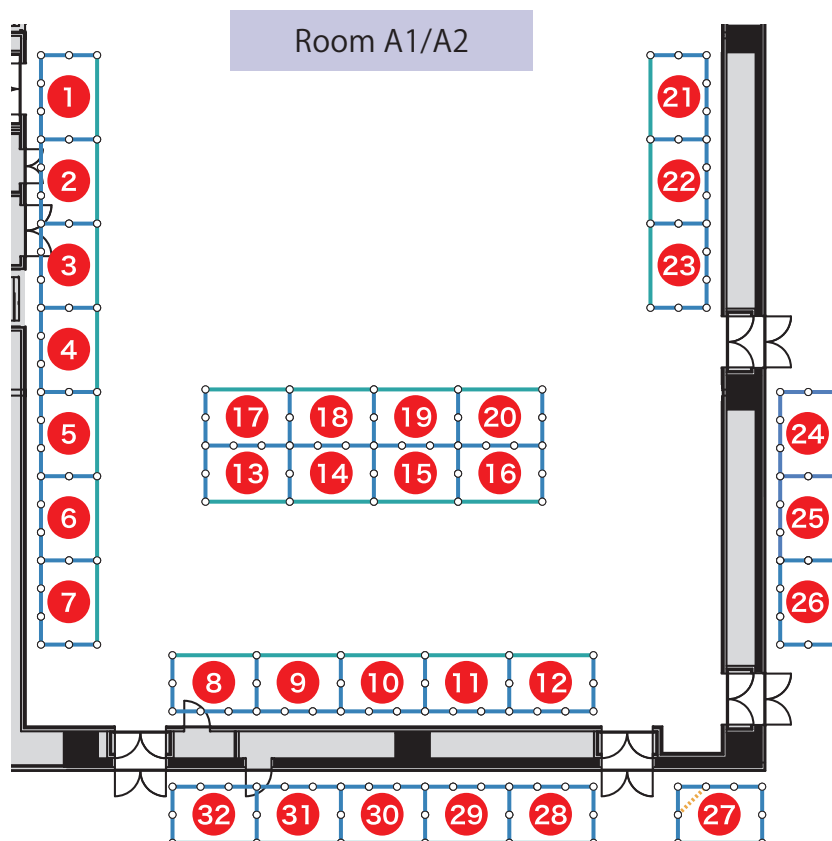
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INDUSTRIAL SESSION

Date: June 1 (Sunday) 17:00-19:00

Venue: Civic Hall; at the 2nd Floor, Kumamoto Jo (Castle) Hall

Session Chair: Dr. Naruhisa Miura, *Mitsubishi Electric Corporation, Japan*

The ISPSD 2025 Industrial Session will be held on Sunday, June 1 from 5PM just after the Short Course. Registered exhibitors will present their latest products and services in 3 minutes. Light refreshments will be served to all participants. So, feel free to come and join us.

Industrial Session Presenters (TBD)

- 1 Silvaco Japan Co., Ltd.
- 2 Orbray Co., Ltd.
- 3 CORNES Technologies Ltd. / SEKI DIAMOND SYSTEMS
- 4 Shanxi Semisic Crystal Co., Ltd.
- 5 Nissin Ion Equipment Co., Ltd.
- 6 MPI Corporation
- 8 ITEST
- 9 Nihon Synopsys G.K.
- 11 TOKAI CARBON CO., LTD.
- 12 ITES Co., Ltd.
- 13 Lam Research Corporation
- 14 Tamura corporation
- 15 Novel Crystal Technology
- 16 NuFlare Technology, Inc.
- 17 Mitsubishi Electric Corporation
- 18 MIRISE Technologies Corporation
- 19 Toray Research Center, Inc.
- 20 AOI ELECTRONICS CO.,LTD.
- 21 Hitachi Hi-Tech Corporation
- 23 SCREEN Semiconductor Solutions Co., Ltd.
- 26 Device Dynamics Lab
- 29 Suzhou HanHua Semiconductor Co.,Ltd
- 30 Ceramicforum Co., Ltd. / Aehr Test Systems
- 31 Beneq Oy
- 32 Epiworld International Co.,Ltd

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ISPSD is the premier forum for technical discussions in all areas of power semiconductor devices and power integrated circuits, including but not limited to device physics, modeling, design, fabrication, materials, packaging and integration, device reliability, and device/circuit interactions.

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Conference Submission Tracks:

- **High Voltage Devices (HV):** High voltage silicon based discrete devices (>200V) such as SJ-MOSFETs, IGBTs, thyristors and pn-diodes
- **Low Voltage Devices and Power IC Device Technology (LVT):** Low voltage silicon based discrete power devices ($\leq 200V$) and devices for power ICs of all voltage ranges
- **Power IC Design (ICD):** Circuit design and demonstration using power IC technology platform
- **GaN and Compound Materials:** GaN and nitride-based compound materials (e.g. AlN, GaAs) based power devices, technology and integration, materials, and processing.
- **SiC and Other Materials (SiC):** SiC and other material (e.g. Ga_2O_3 , diamond) based power devices, technology and integration, materials, and processing.
- **Module and Packaging Technologies (PK):** System Integration in Package Module and package technology for discrete power devices and power ICs

Abstract Submission

Prospective authors should visit the ISPSD 2026 website: <https://www.ispsd2026.com>

Important Dates:

Jan 19, 2026: **4-pages full paper** submission
March 2, 2026: Author notification
March 16, 2026: Final submission deadline for final paper and copyright filing

Please Note: ISPSD 2026 has changed the paper submission process. Note that a 4-page full paper submission is required. Traditional "Abstract Submission" will NOT be accepted. No late news session.

Template:

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Paper length: Maximum 4 pages

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General Chair:

Dr. David Sheridan
Alpha & Omega Semiconductor
USA Email: David.sheridan@us.aosmd.com

Technical Program Chair:

Dr. Sameh Khalil
Infineon Technologies
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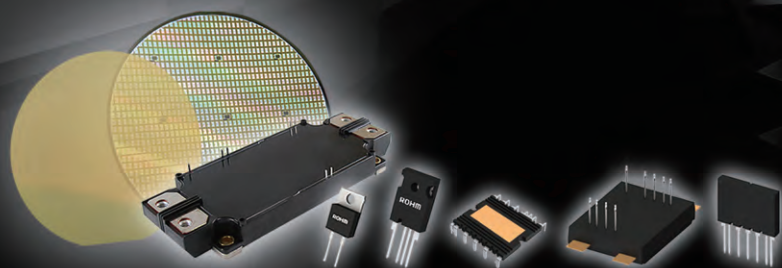




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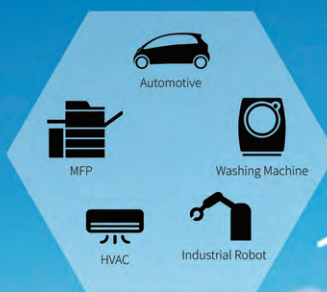
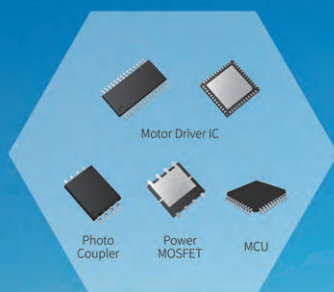
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SCHEDULE AT A GLANCE

Time	June 1 Sun	June 2 Mon	June 3 Tue	June 4 Wed	June 5 Thu
8:30	Short Course Opening	8:30 - 9:00 Opening Session			
9:00	8:40 - 9:30 Short Course 1		8:40 - 10:20 LVT Low Voltage Power Devices	8:40 - 10:20 SiC-4 Gallium Oxide and Diamond Devices	8:40 - 10:20 HV-2 Multi-Gate Technology and SJ Devices
9:30	9:30 - 10:20 Short Course 2	9:00 - 10:20 Plenary Session			
10:00	10:20 - 10:50 Coffee	10:20 - 10:50 Coffee	10:20 - 10:50 Coffee	10:20 - 10:50 Coffee	10:20 - 10:50 Coffee
10:30	10:50 - 11:40 Short Course 3	10:50 - 12:30 HV-1 New Power Device Designs and Gate Control Method	10:50 - 12:30 ICD Power IC Design	10:50 - 12:30 SiC-2 Design Approaches and Physics for Reliability and Performance of SiC Devices	10:50 - 12:30 SiC-3 Novel Devices and Ruggedness of SiC
11:00					
11:30	11:40 - 12:30 Short Course 4				
12:00					
12:30	12:30 - 14:00 Lunch	12:30 - 14:00 Lunch	12:30 - 14:00 Lunch	12:30 - 14:00 Lunch	12:30 - 14:00 Lunch
13:00					
13:30					
14:00	14:00 - 14:50 Short Course 5	14:00 - 15:40 SiC-1 Performance of Superjunction SiC devices	14:00 - 15:20 GaN-2 GaN Power Device Reliability and Tests	14:00 - 15:40 PK Packaging Technologies	14:00 - 15:20 GaN-3 Novel GaN Power Device and Technologies 2
14:30					
15:00	14:50 - 15:40 Short Course 6		15:20 - 15:40 Coffee		15:20 - 15:50 Closing Session
15:30	15:40 - 16:30 Short Course 7	15:40 - 16:10 Coffee		15:40 - 16:00 Coffee	
16:00		16:10 - 17:50 GaN-1 Novel GaN Power Device and Technologies 1	15:40 - 17:40 Poster Session 1 LVT/ICD/GaN	16:00 - 18:00 Poster Session 2 HV/PK/SiC	
16:30	16:30 - 17:00 Coffee				
17:00	17:00 - 19:00 Industrial Session				
17:30					
18:00					
18:30					
19:00		Welcome Reception	AdCom Meeting (Invitation Only)	Banquet Hall of Fame	TPC Meeting (Invitation Only)
19:30					
20:00					
20:30					
21:00					

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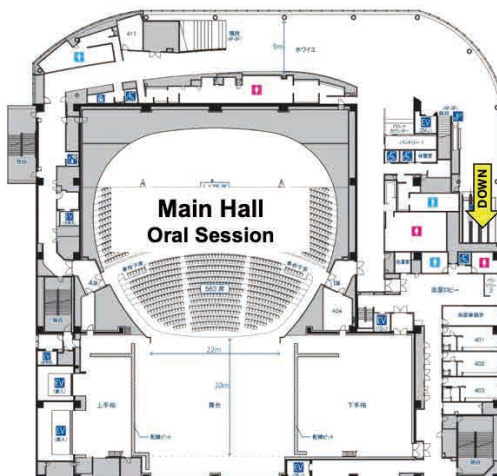


WiFi

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